National Taiwan University

Fabrication Processes

半導體及微奈米機電製程概述

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你知道什麼是半導體嗎?什麼是積體電路嗎?

你知道什麼是微奈米機電(MEMS or NEMS)嗎?

微機電為什麼又叫微奈米機電(MEMS or NEMS)呢?

Outline

- Introduction to MEMS Technologies
- Clean room
- Silicon Wafers
- Photolithography
- Film Vapor Deposition
- Silicon Etching Technique
- Conclusions

Introduction to MEMS Technologies

Introduction (1) — Father of MEMS

- 理查·費曼的演講
- 1959年，美國物理學會年會演講

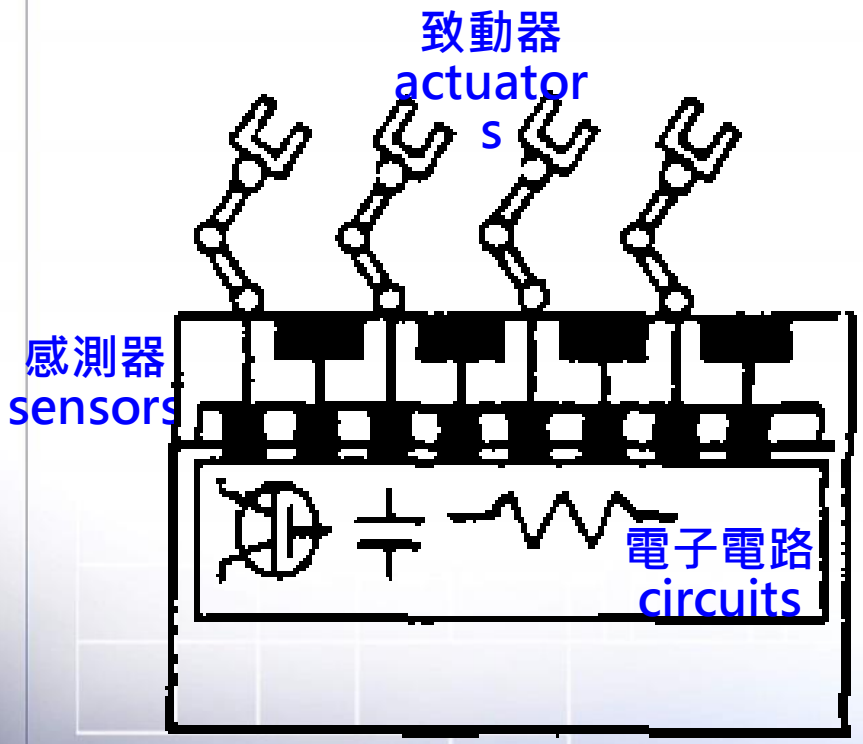
「There is plenty of room at the bottom」
底下的空間還大的很

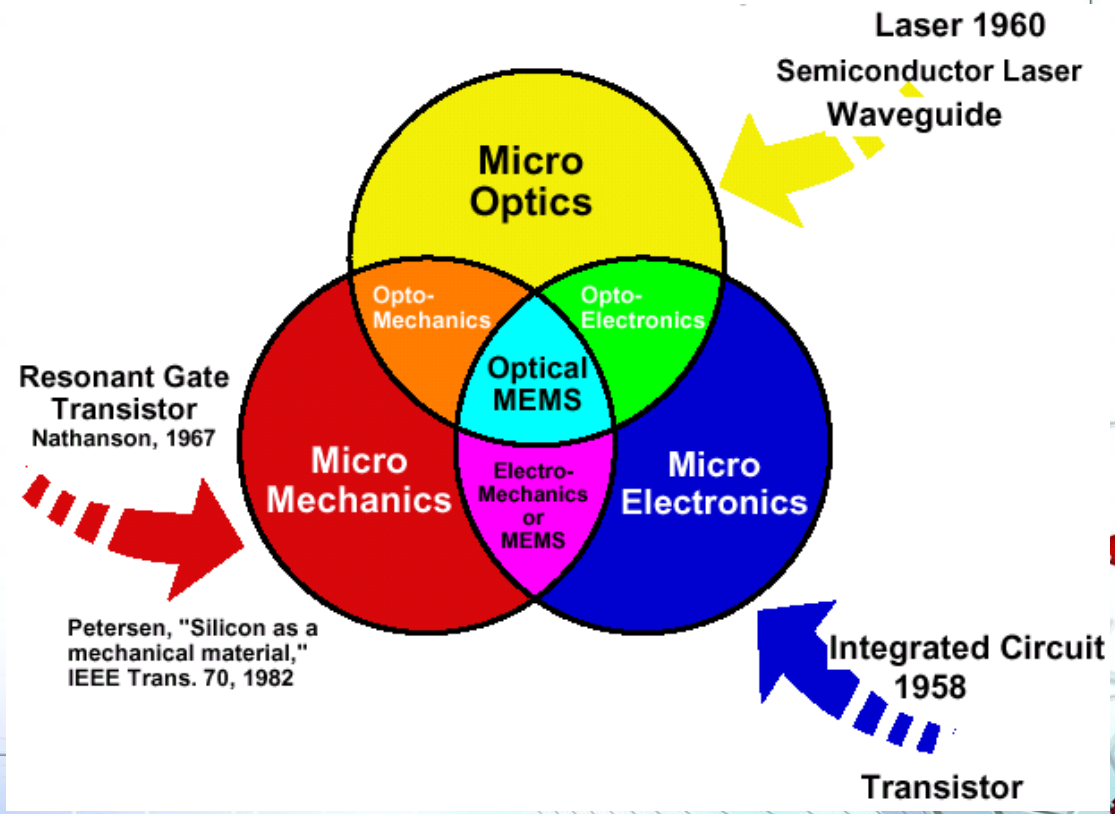
- 書本上的字句縮小25,000倍

理查·費曼

微機電系統技術的發展背景

- 微機電系統技術起源於1960年代對積體電路的研究
- 發展的理念在於如何將電子電路微小化
- 科技人員改善傳統加工技術及應用半導體製程，試圖將各種機械元件微小化，進而產生微機電系統技術





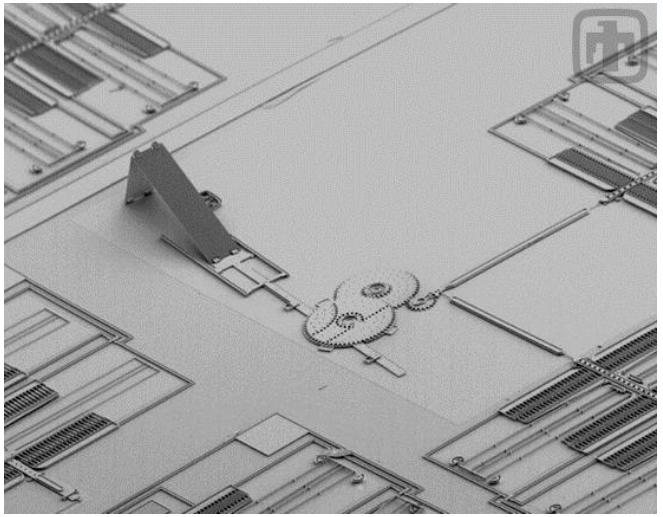
Introduction (2) — What's MEMS ?

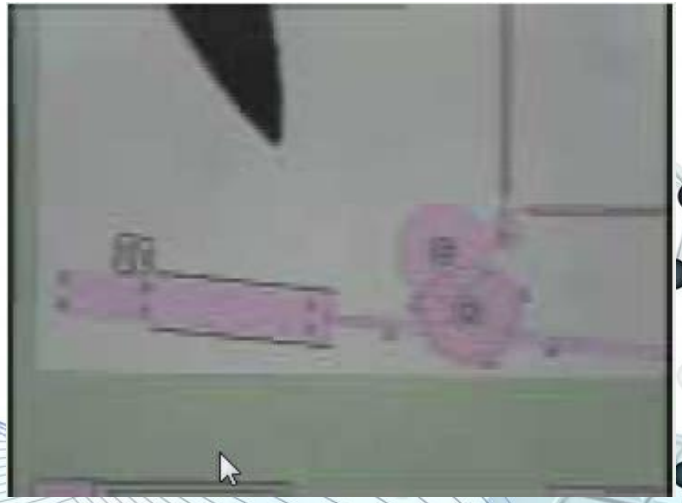
微機電系統名稱分類

美　國：**Micro-Electro-Mechanical System (MEMS)**

日　本：**Micromachines**

歐　洲：**Micro-Systems Technology (MST)**





Sandia National Lab., USA

Introduction (3) — MEMS Technologies

微機電系統產品的優點

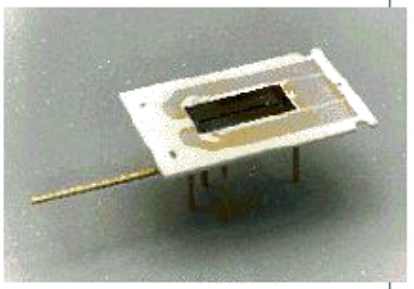
- 超「輕、薄、短、小」
- 高附加價值
- 符合環保、省能源
- 省空間、省材料等

質譜儀

70 Kg, 30000 cm^3, 1200 W

Europa Scientific, UK

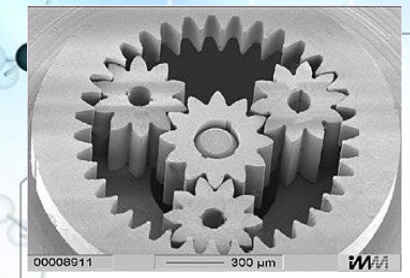
微機電系統技術



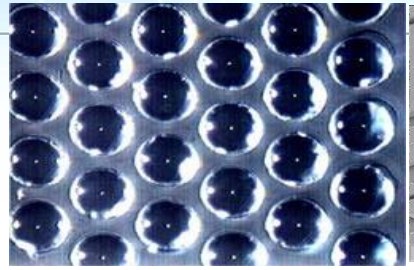
微質譜儀晶片

0.2 Kg, 3 cm^3, 0.5 W

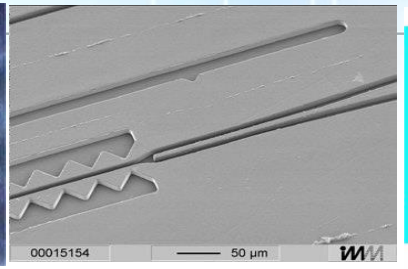
DARPA, USA



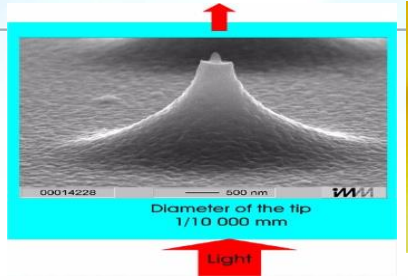
(a) 微齒輪組



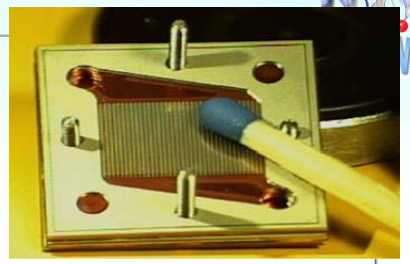
(b) 微鏡片



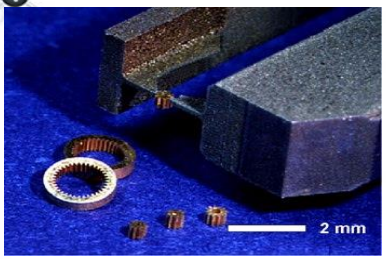
(c) 整合光學分光器



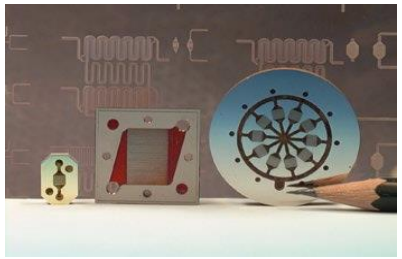
(d)近場光學探針



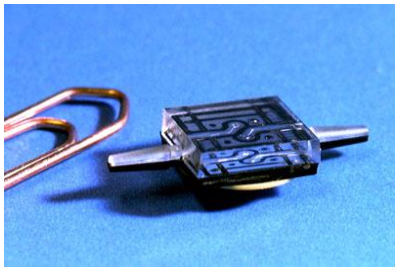
(e) 微熱交換器



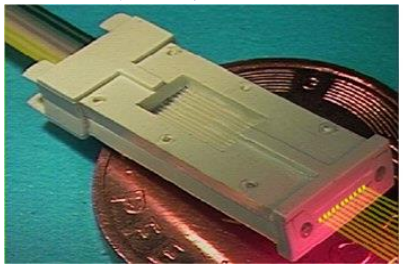
(f) 微組合



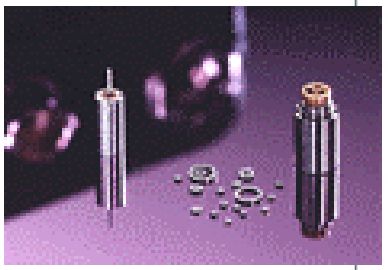
(h) 微幫浦



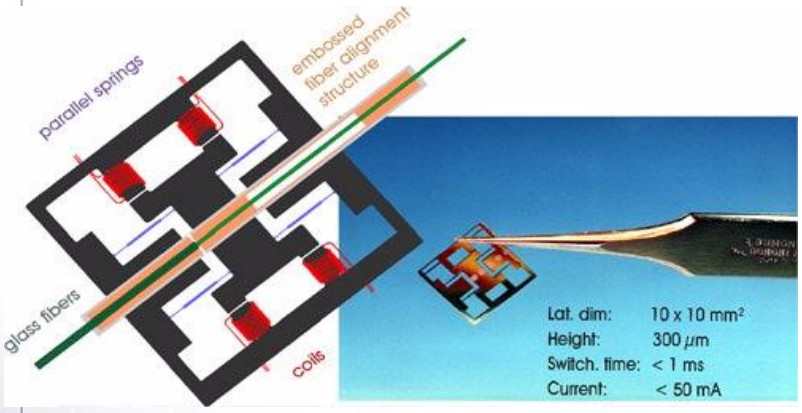
(g) 微反應器



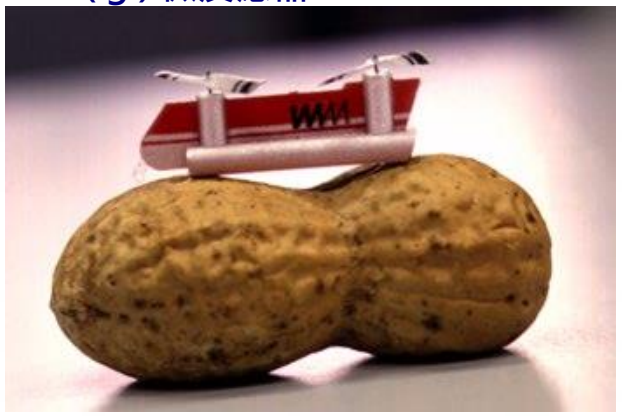
(i) 光纖固定器



(j) 微馬達



(k) 光纖開關



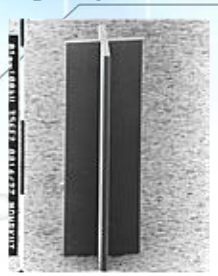
(l) 微小直升機

IMM 微系統研究中心

IMM微系統研究中心所開發的產品

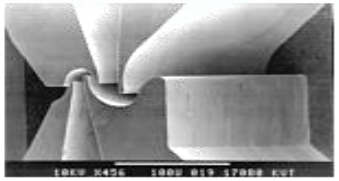
Source: http://www.imm-mainz.de

high aspect ratio

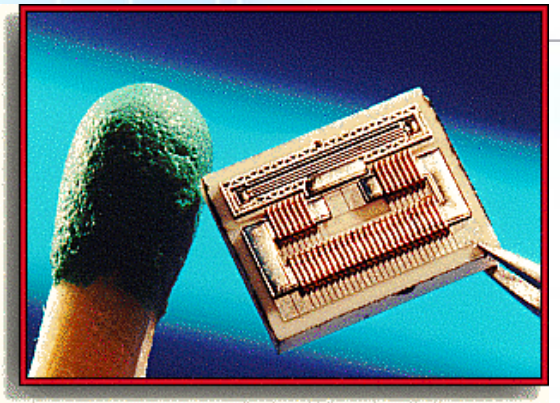


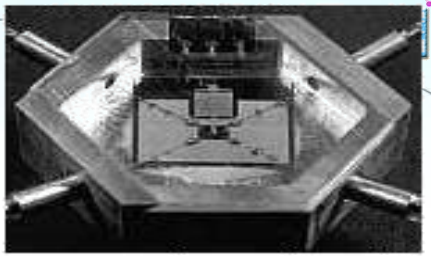
Bar structure 400 µm high, with parallel sidewalls.

any lateral shape

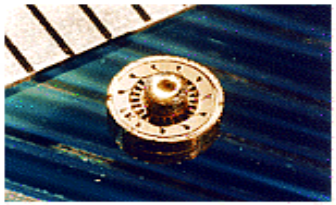


Separation nozzle as an example of arbitrary lateral shaping.

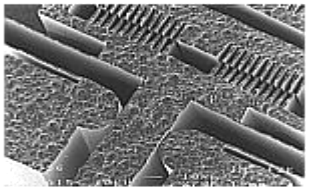




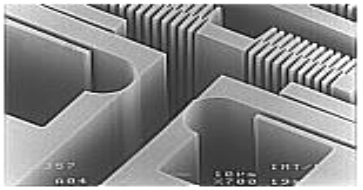
Micro-optical bypass switch with electrostatic actuator for moving a mirror.



Microturbine (Ø = 2.5 mm) for cardiac catheters, power: 40 mW

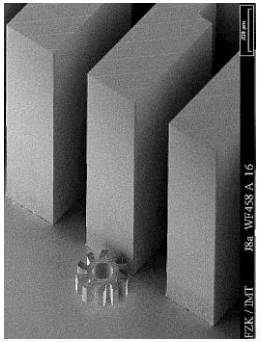


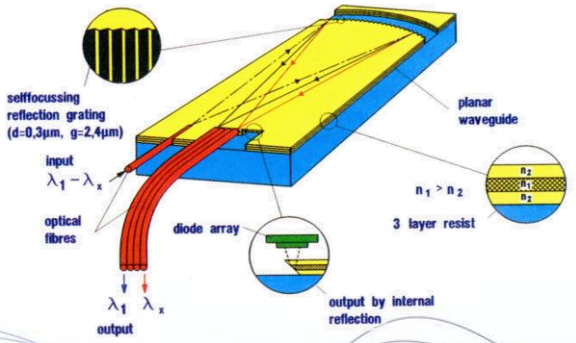
Nickel structure of an electrostatic linear actuator after electroforming and dissolution of the remaining resist parts. The structure height is 80 µm.



Detail of a 100 µm high PMMA structure of an electrostatic linear actuator. The smallest lateral PMMA structure is 1 µm and forms the gap between the conical capacitor plates.

Micromembrane pump from the small series manufactured at the Research Center, as compared to the size of an ant.





IMT微系統研究中心所開發的產品

Source: http://www.fzk.de/imt/eimt

應用

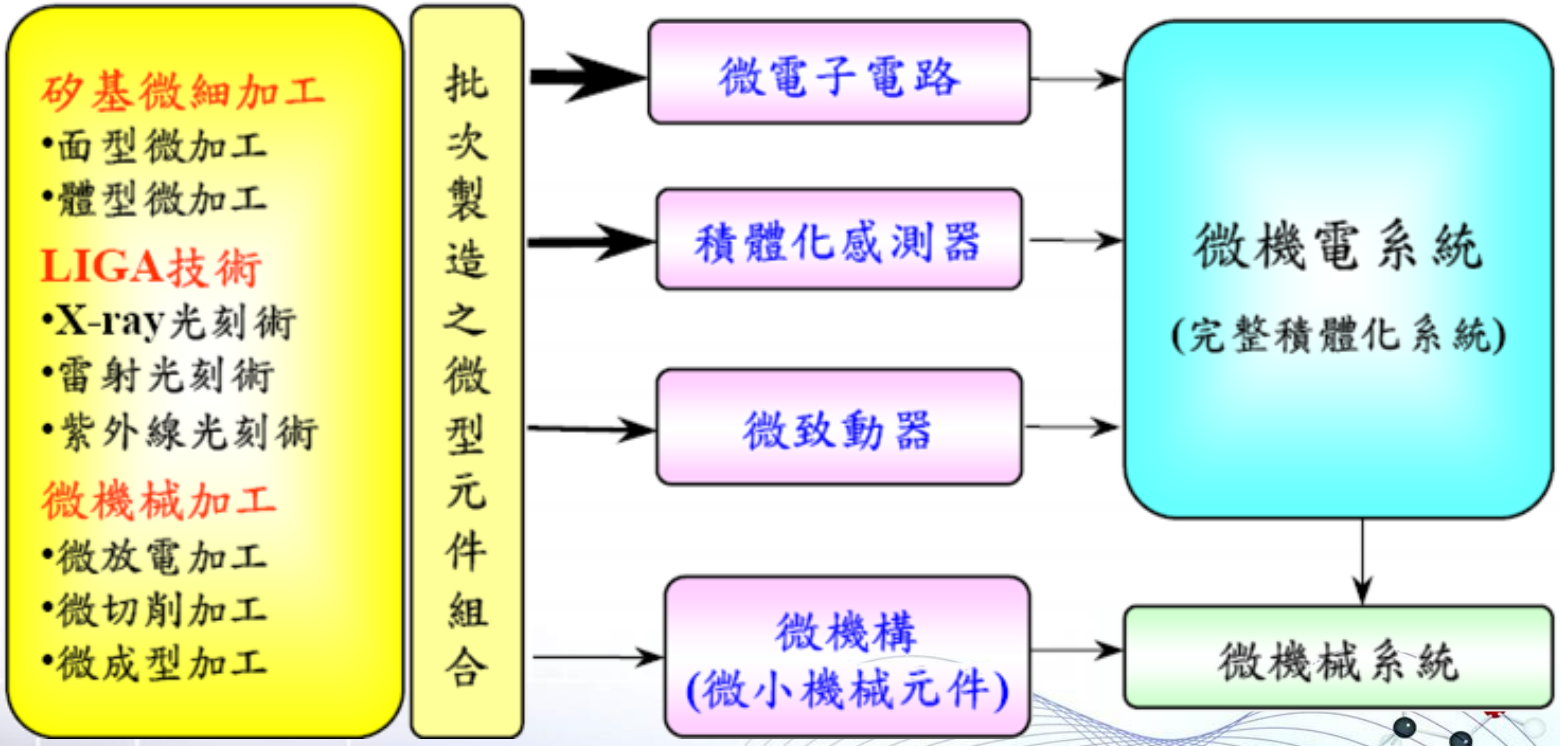
IBM千足計畫 https://www.youtube.com/watch?v=roBC8_OTcuU

生醫感測 https://www.youtube.com/watch?v=E3lWwJF8gl8

Introduction (4) — Definition

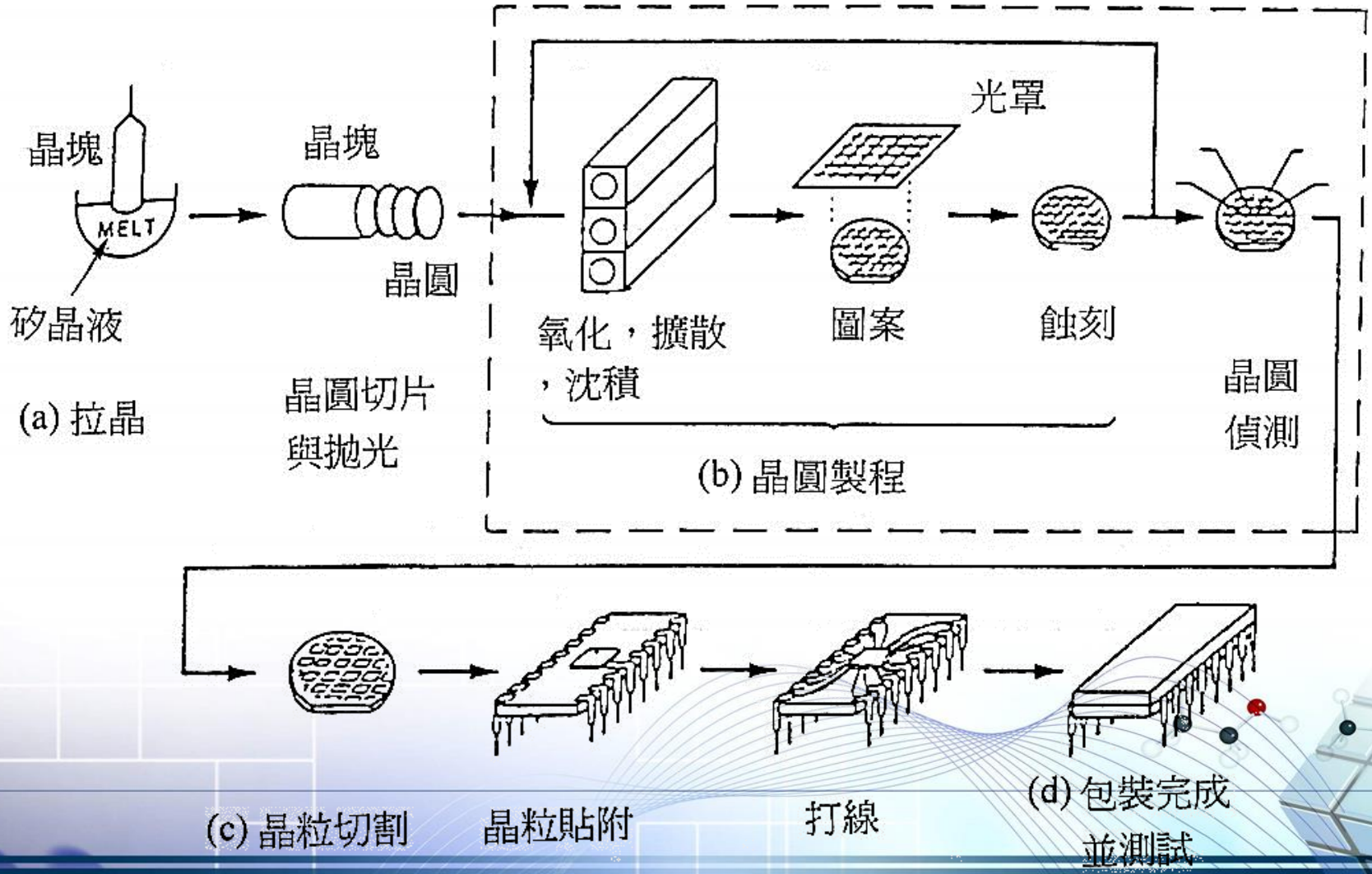
半導體製程:系指利用半導體材料進行積體電路製作之過程

微機電與奈米機電:應用於微米(um)10-6m與奈米(nm)10-9加工技術研製微細元件及組件，並整合微電子電路與微控制器



Introduction (5) — IC

半導體IC製造流程



Clean room

Clean room (1) — Background

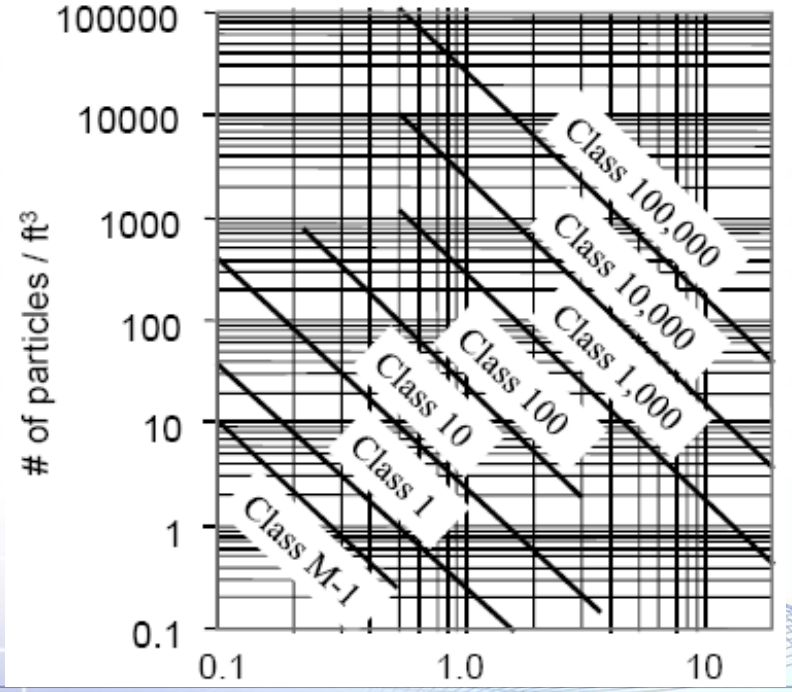
- **Artificial environment with low particle counts**
- **Started in medical application for post-surgery infection prevention**
- **Particles kills yield**
- **IC and MEMS fabrication must in a clean room**

Clean room (2) — Background

- First used for surgery room to avoid bacteria contamination
- Adopted in semiconductor industry in 1950
- Smaller device needs higher grade clean room
- Less particle, more expensive to build

Clean room (3) — Clean Room Class

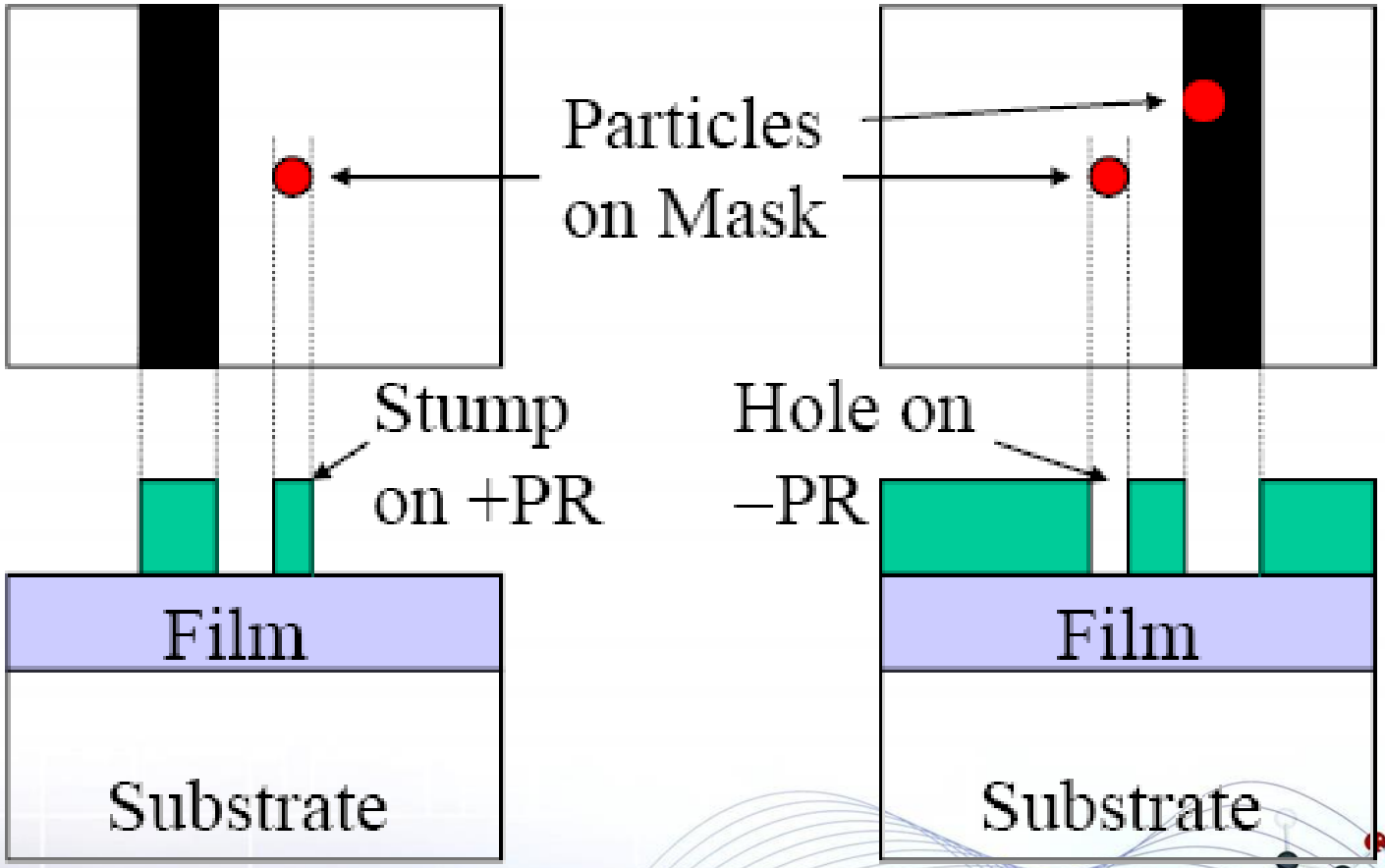
- **Class 10 is defined as less than 10 particles with diameter larger than 0.5 µm per cubic foot.**
- **Class 1 is defined as less than 1 such particles per cubic foot.**
- **0.18 µm device require higher than Class 1 grade clean room.**



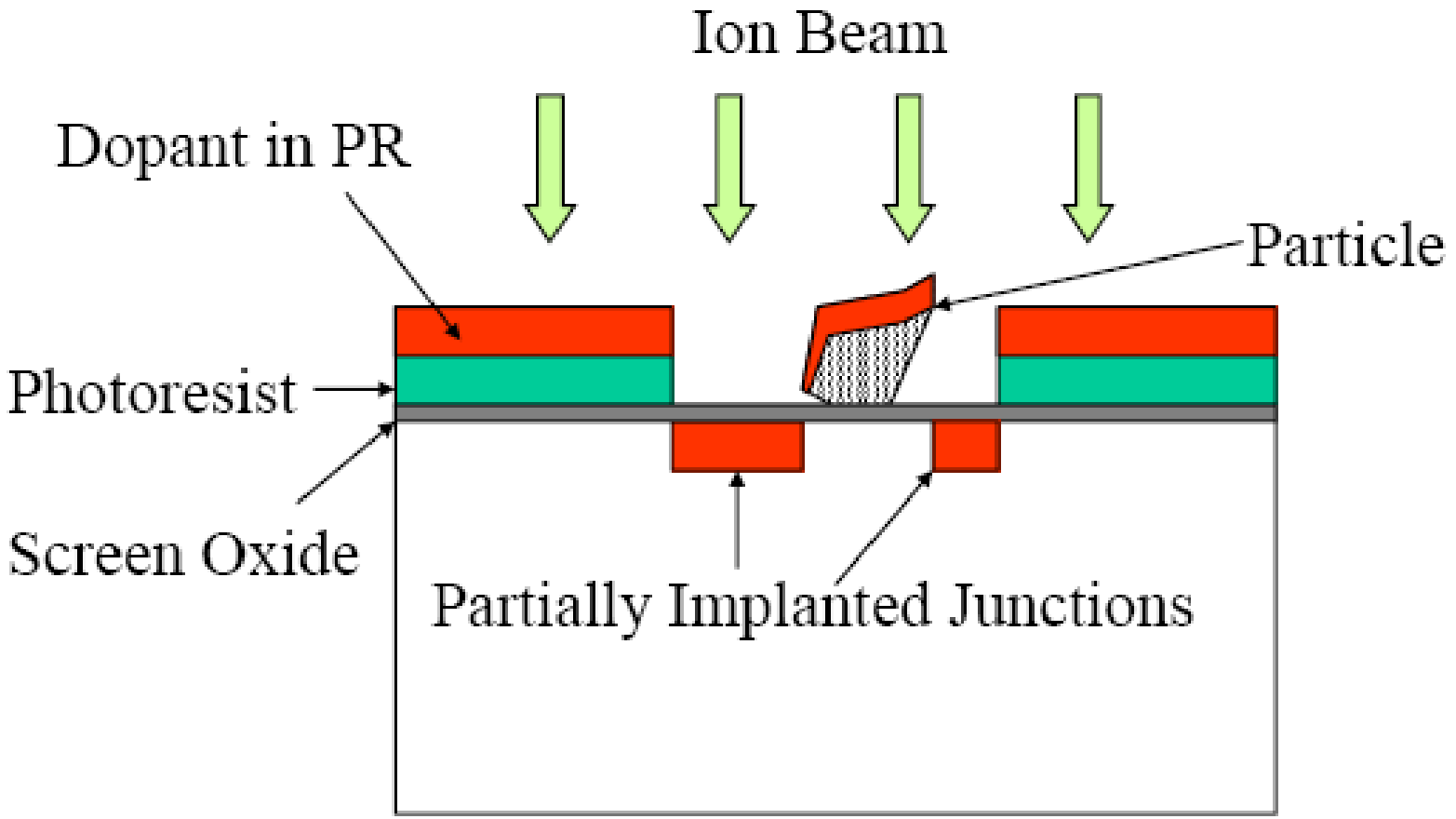
Clean room (4) — Definition of Airborne Particulate Cleanliness Class

Class	Particles/ft^3				
	0.1 µm	0.2 µm	0.3 µm	0.5 µm	5 µm
M-1	9.8	2.12	0.865	0.28	
1	35	7.5	3	1	
10	350	75	30	10	
100		750	300	100	
1000				1000	7
10000				10000	70

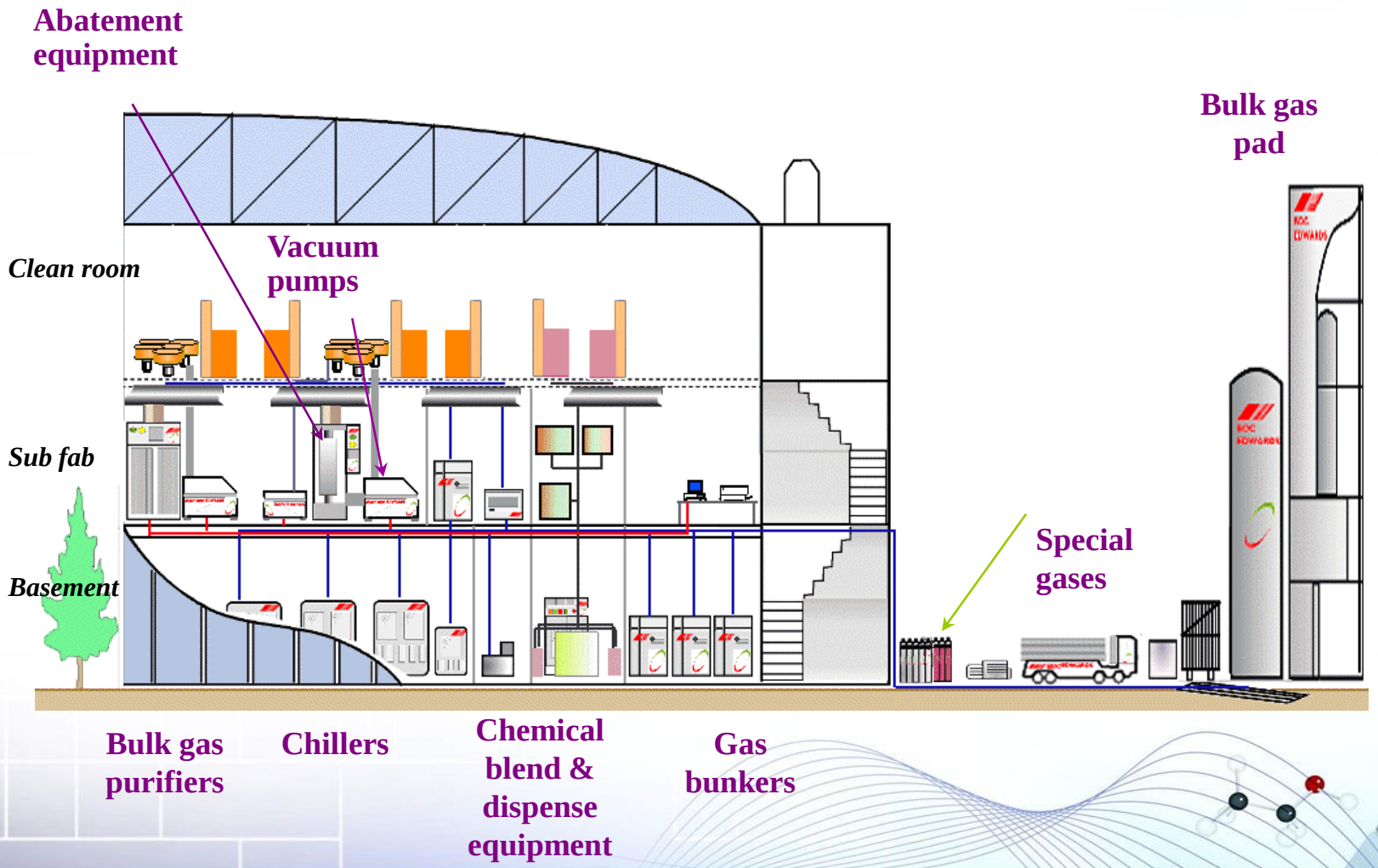
Clean room (5) — Effect of Particles on Masks

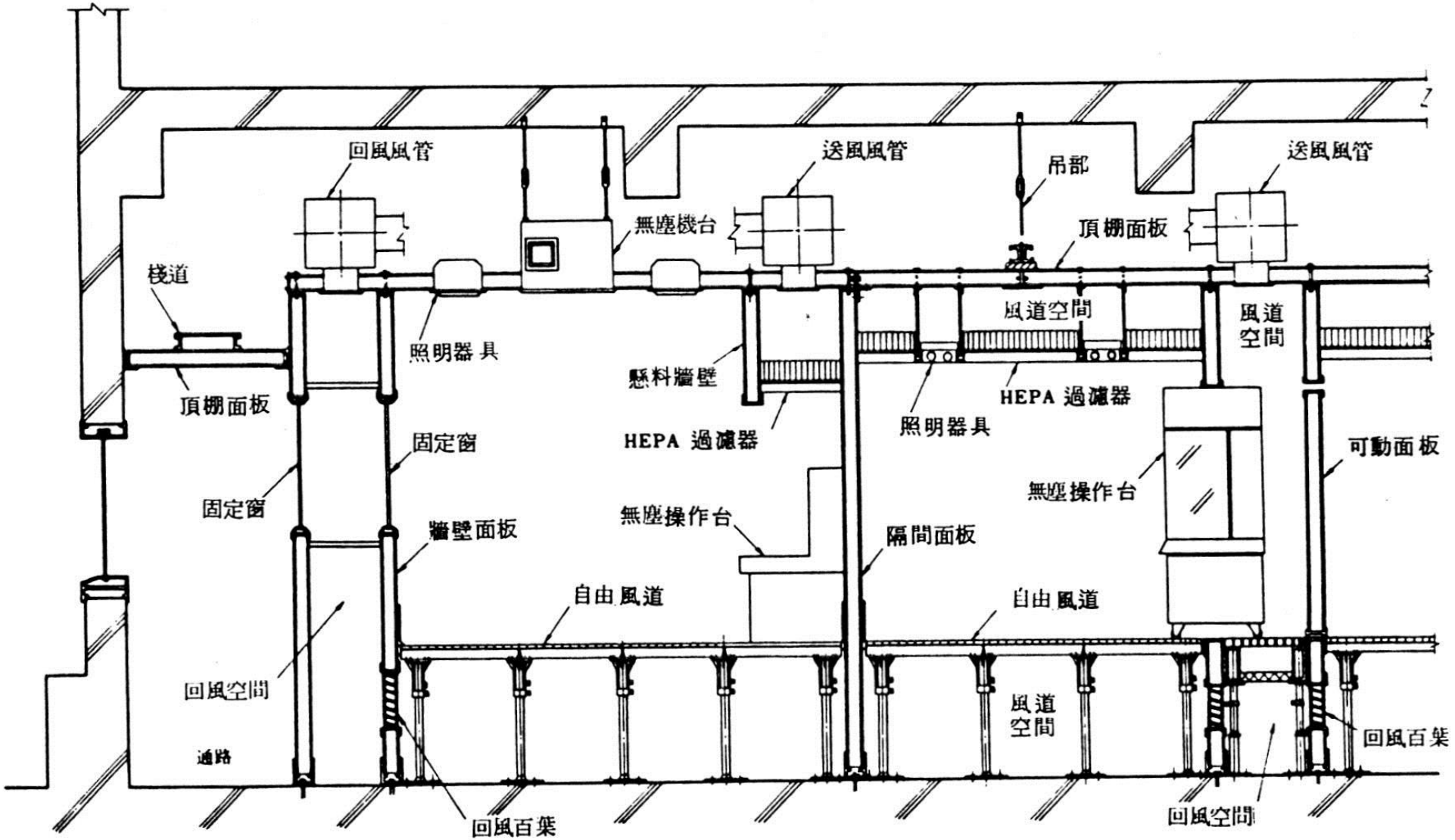


Clean room (6) — Effect of Particle Contamination



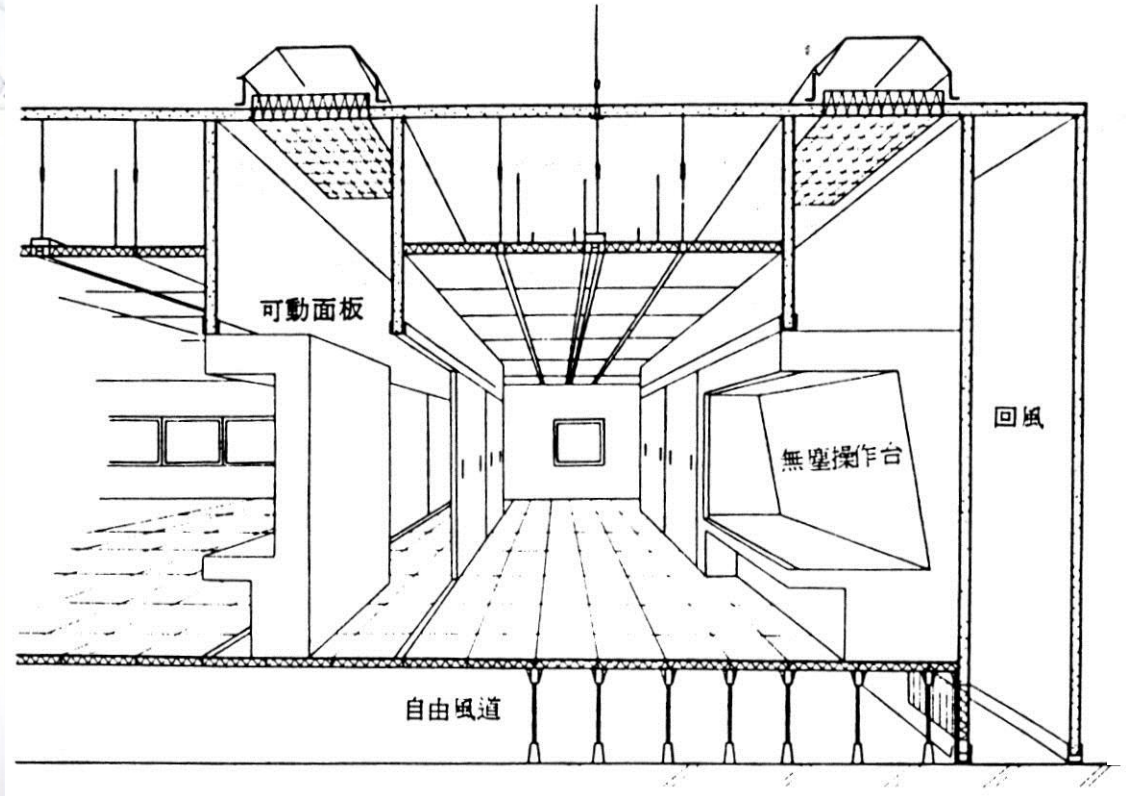
Clean room (6) — 無塵室(Clean room or FAB)之構成

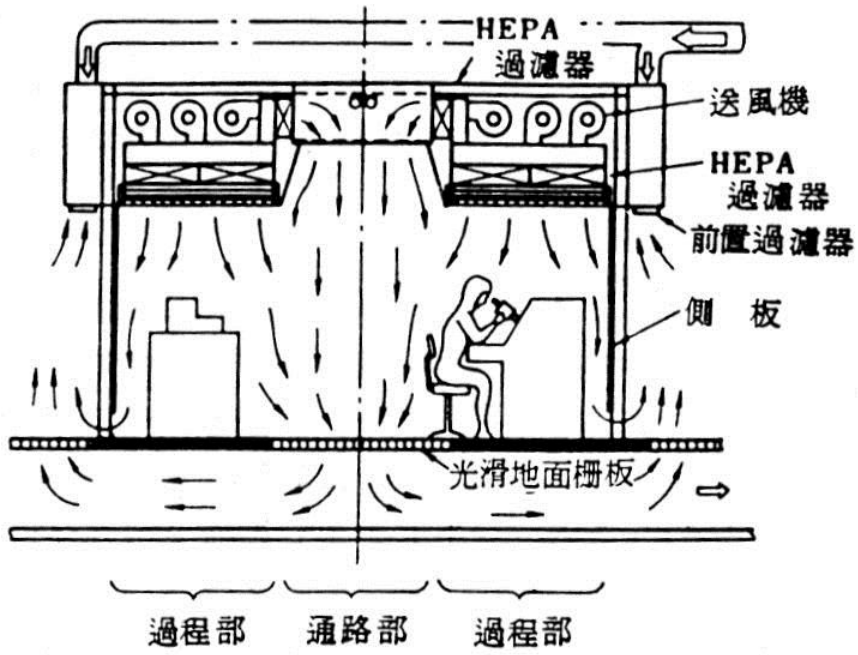



回風風管
送風風管
吊部
送風風管
無塵機台
頂棚面板
棧道
風道空間
風道
空間
照明器具
懸料牆壁
HEPA 過濾器
頂棚面板
照明器具
HEPA 過濾器
固定窗
可動面板
固定窗
無塵操作台
牆壁面板
無塵操作台
隔間面板
自由風道
自由風道
回風空間
風道
空間
回風百葉
通路
回風百葉
回風空間

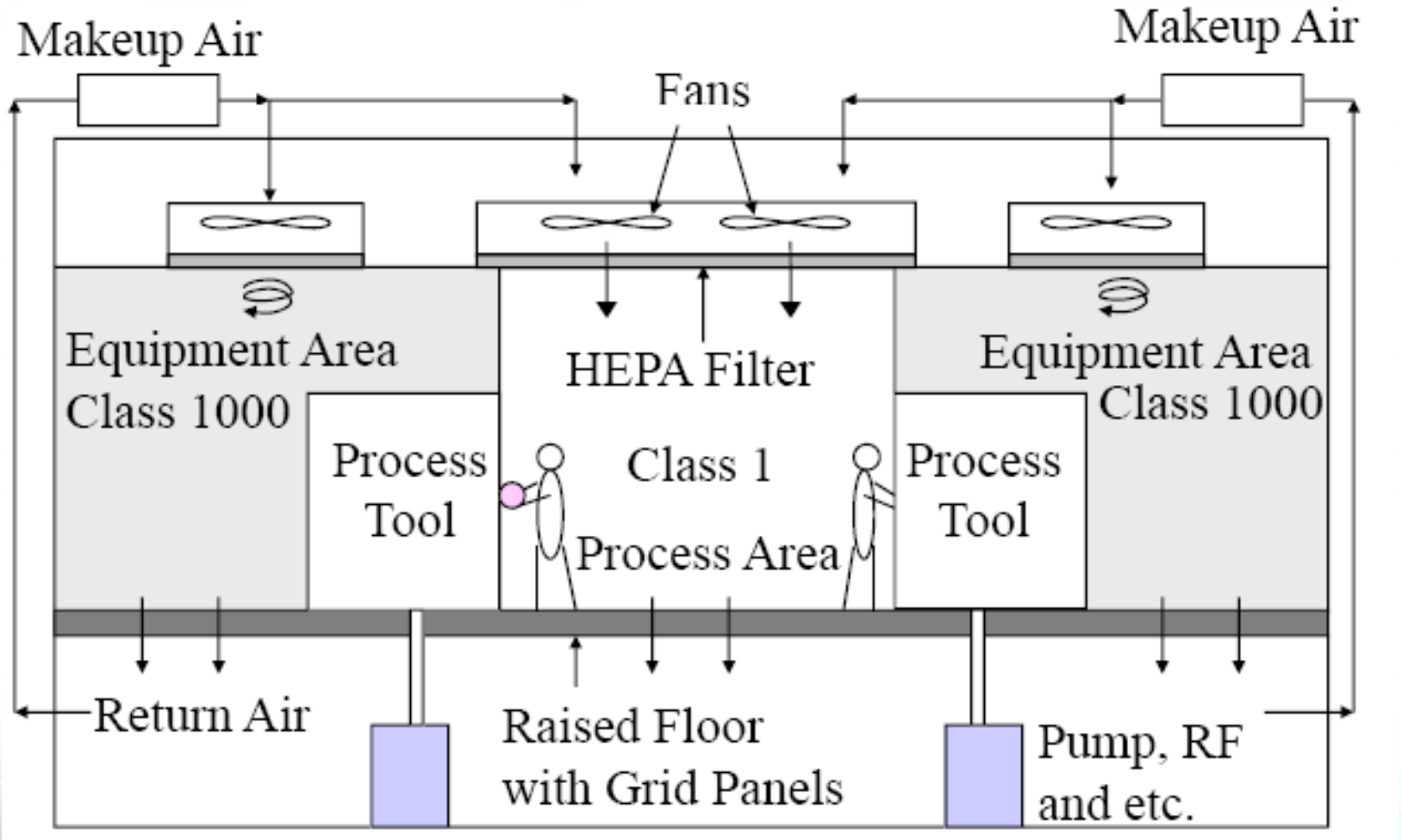
無塵室縱斷面圖

Clean room (7) — 無塵室之構成(續)





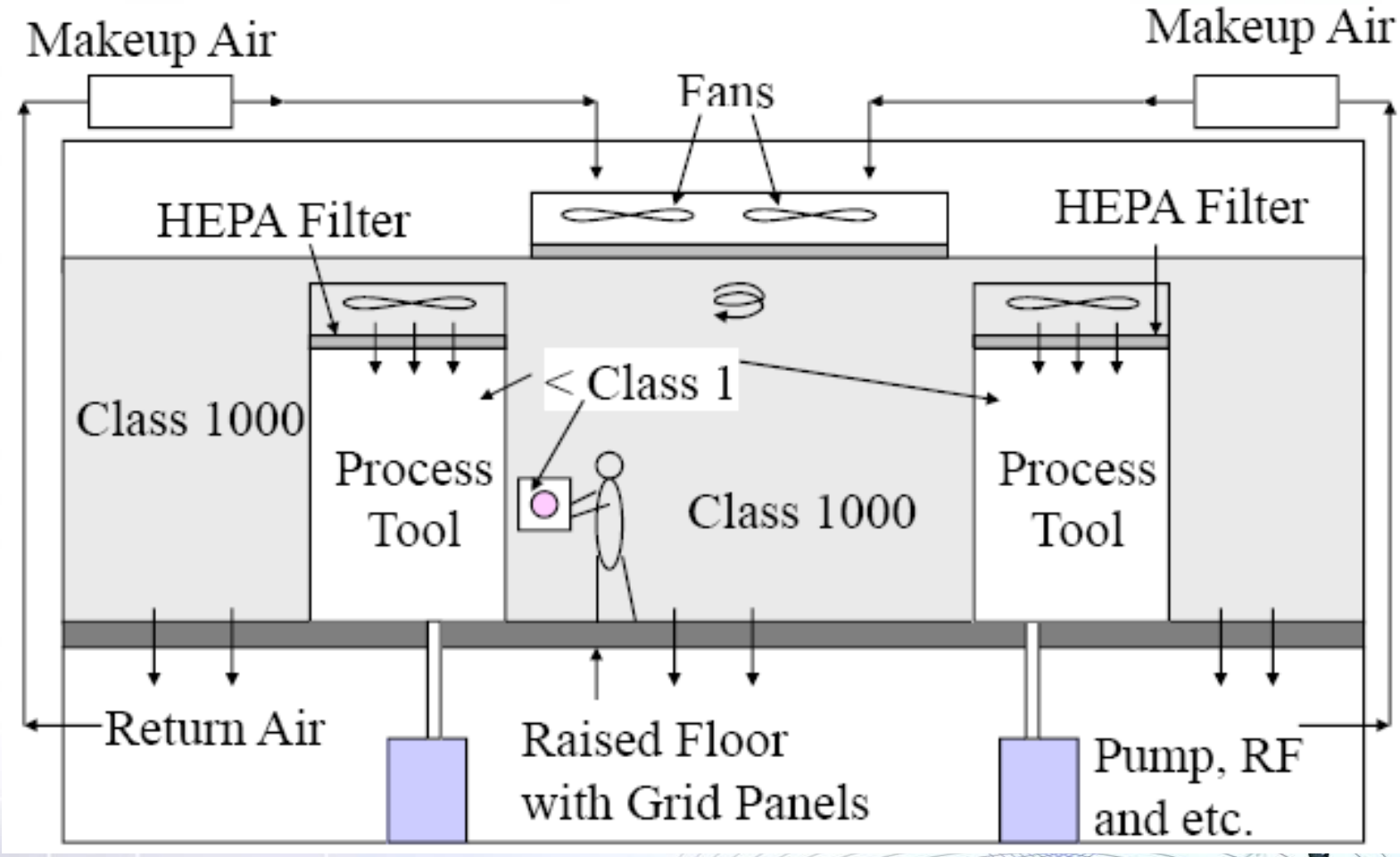
Clean room (8) — Cleanroom Structure



Clean room (9) — Mini-environment

- **Class 1000 cleanroom, lower cost**
- **Boardroom arrangement, no walls between process and equipment**
- **Better than class 1 environment around wafers and the process tools**
- **Automatic wafer transfer between process tools**

Clean room (10) — Mini-Environment Cleanroom

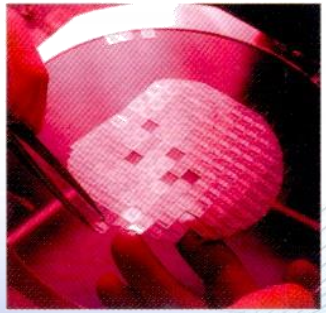


無塵實驗室與生產工廠

無塵實驗室與生產工廠

實現微/奈米元件的場所

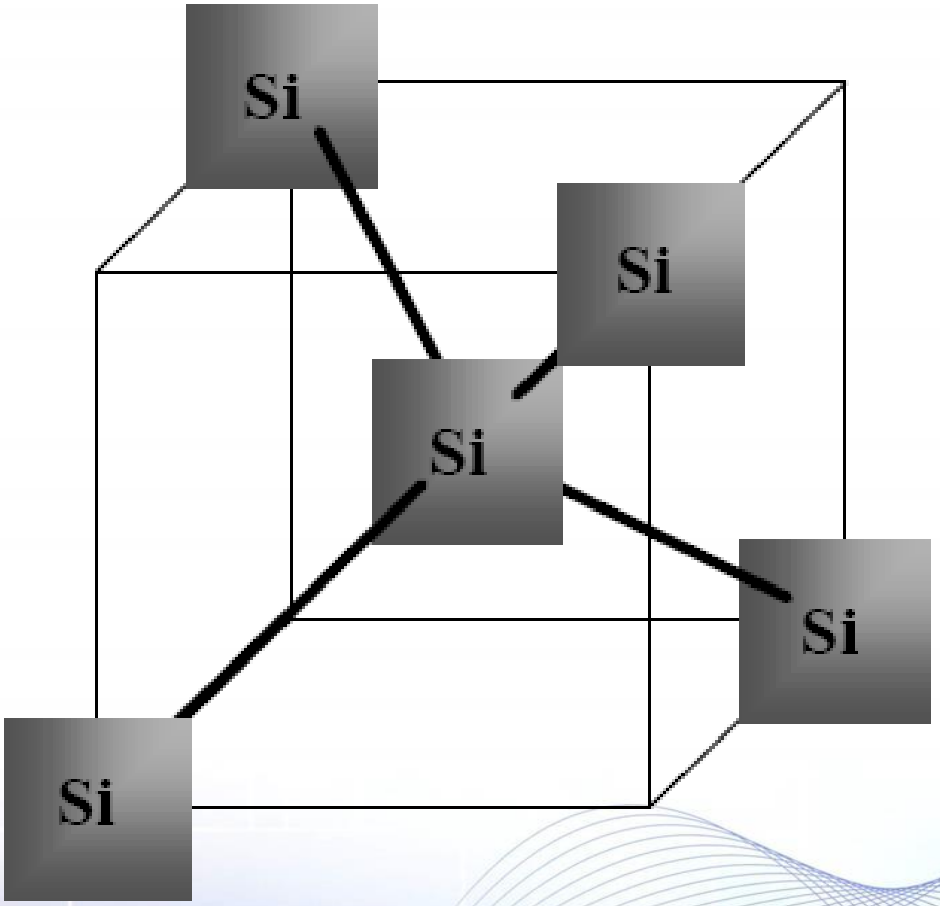
Silicon Wafers



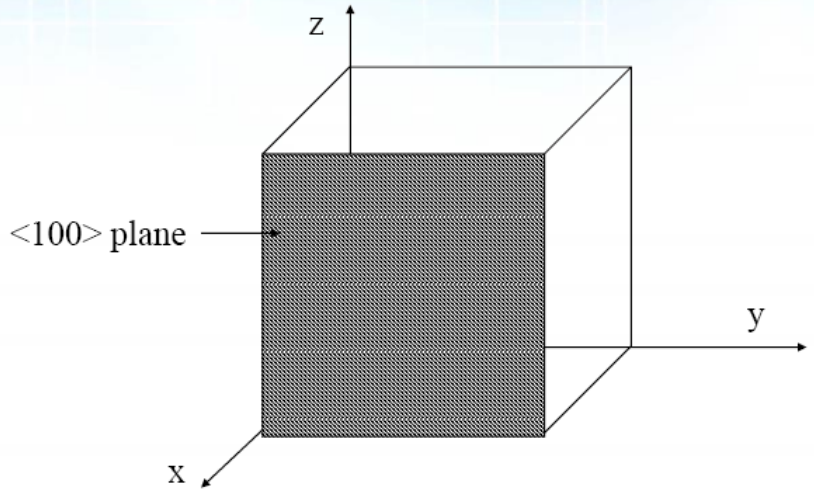
Silicon Wafers (1) — Why Silicon?

- **Abundant, inexpensive**
- **Thermal stability**
- **Silicon dioxide is a strong dielectric and relatively easy to form**
- **Silicon dioxide can be used as diffusion doping and etch mask**

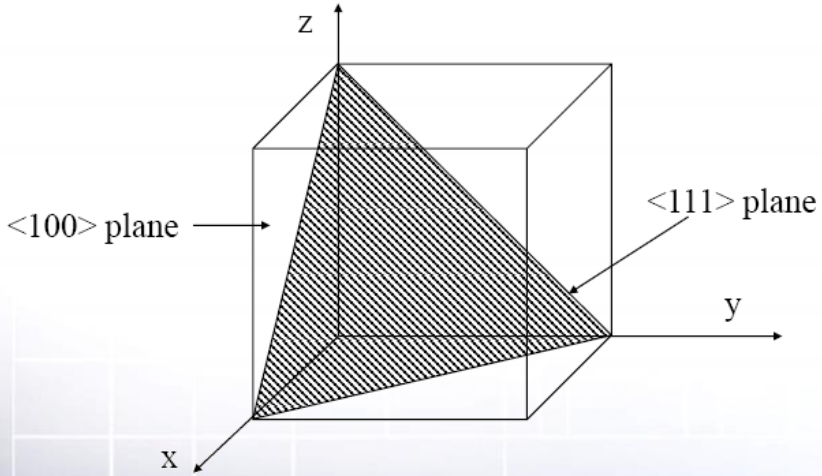
Silicon Wafers (2) — Unit Cell of Single Crystal Silicon



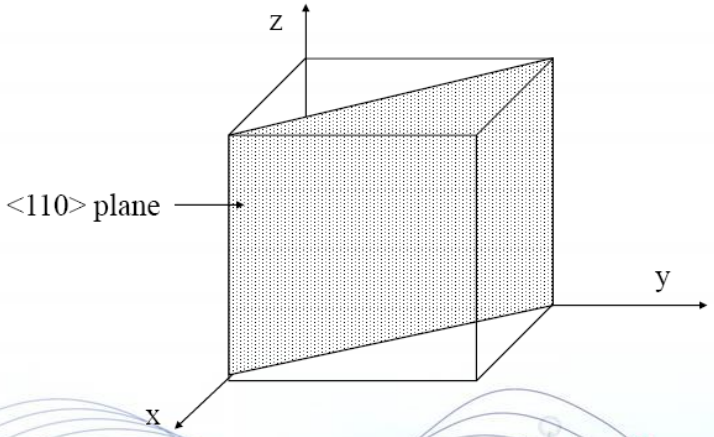
Crystal Orientations: <100>



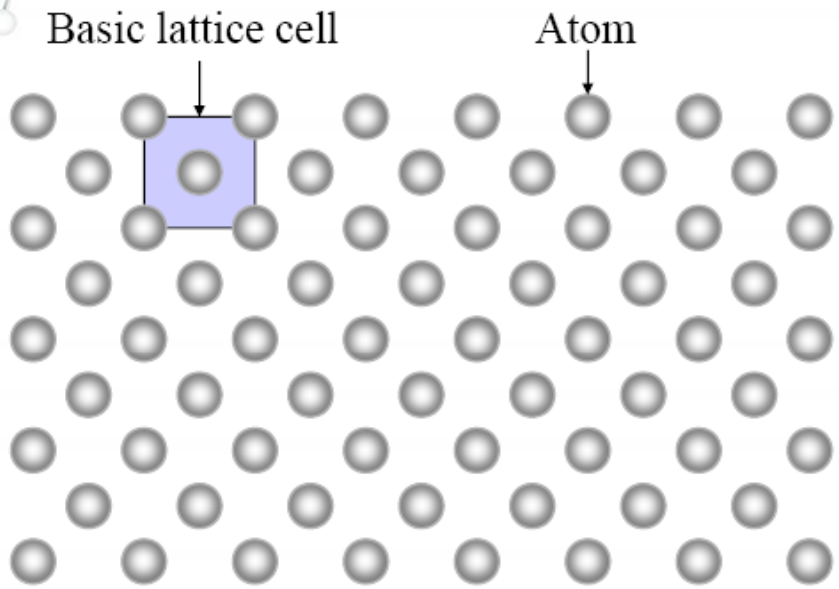
Crystal Orientations: <111>



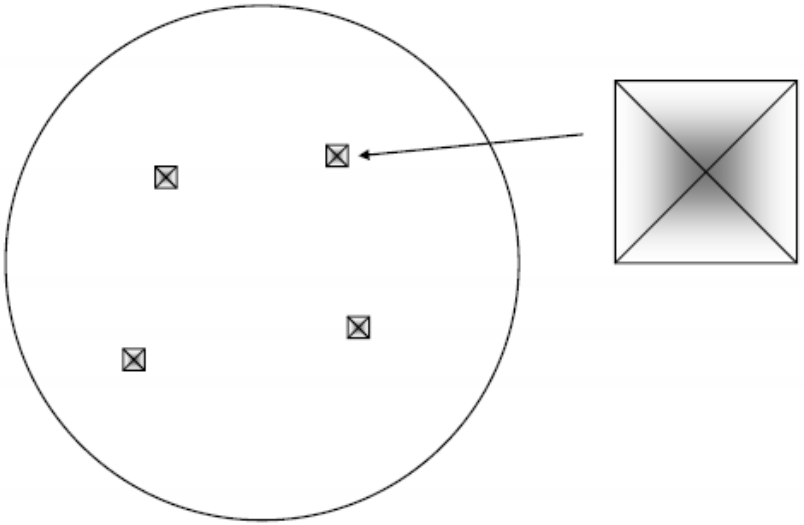
Crystal Orientations: <110>



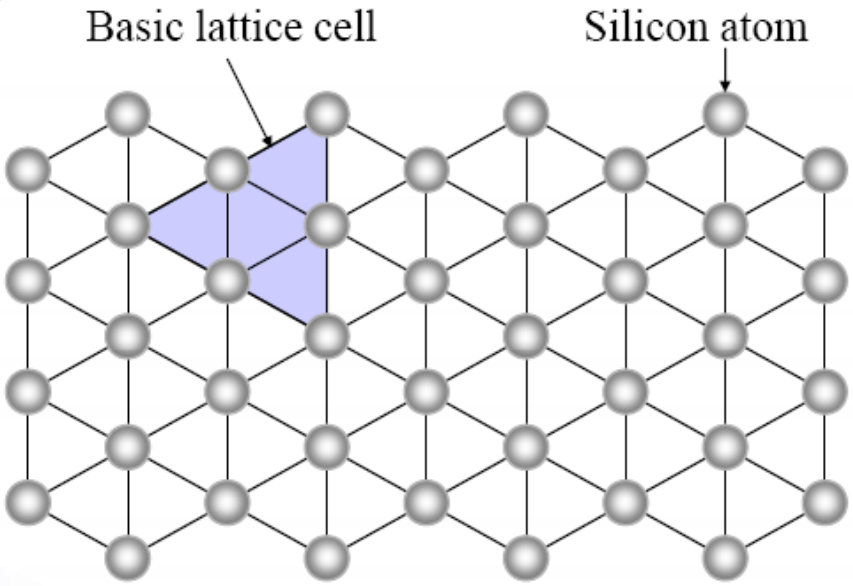
<100> Orientation Plane



<100> Wafer Etch Pits



<111> Orientation Plane



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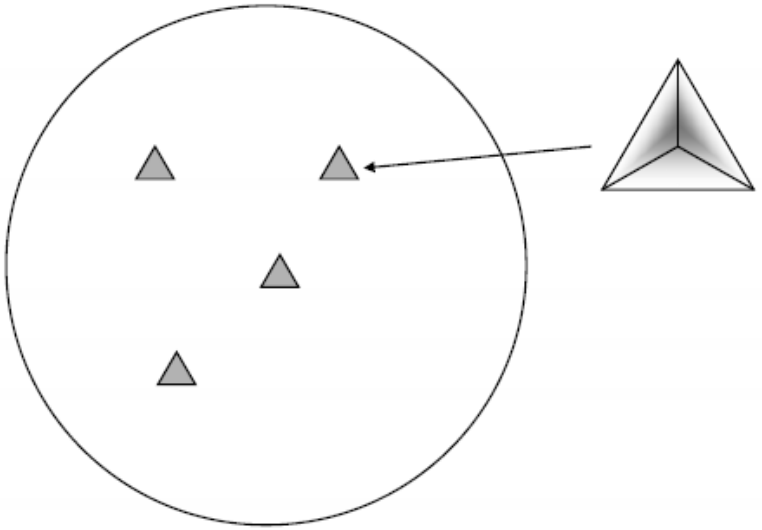
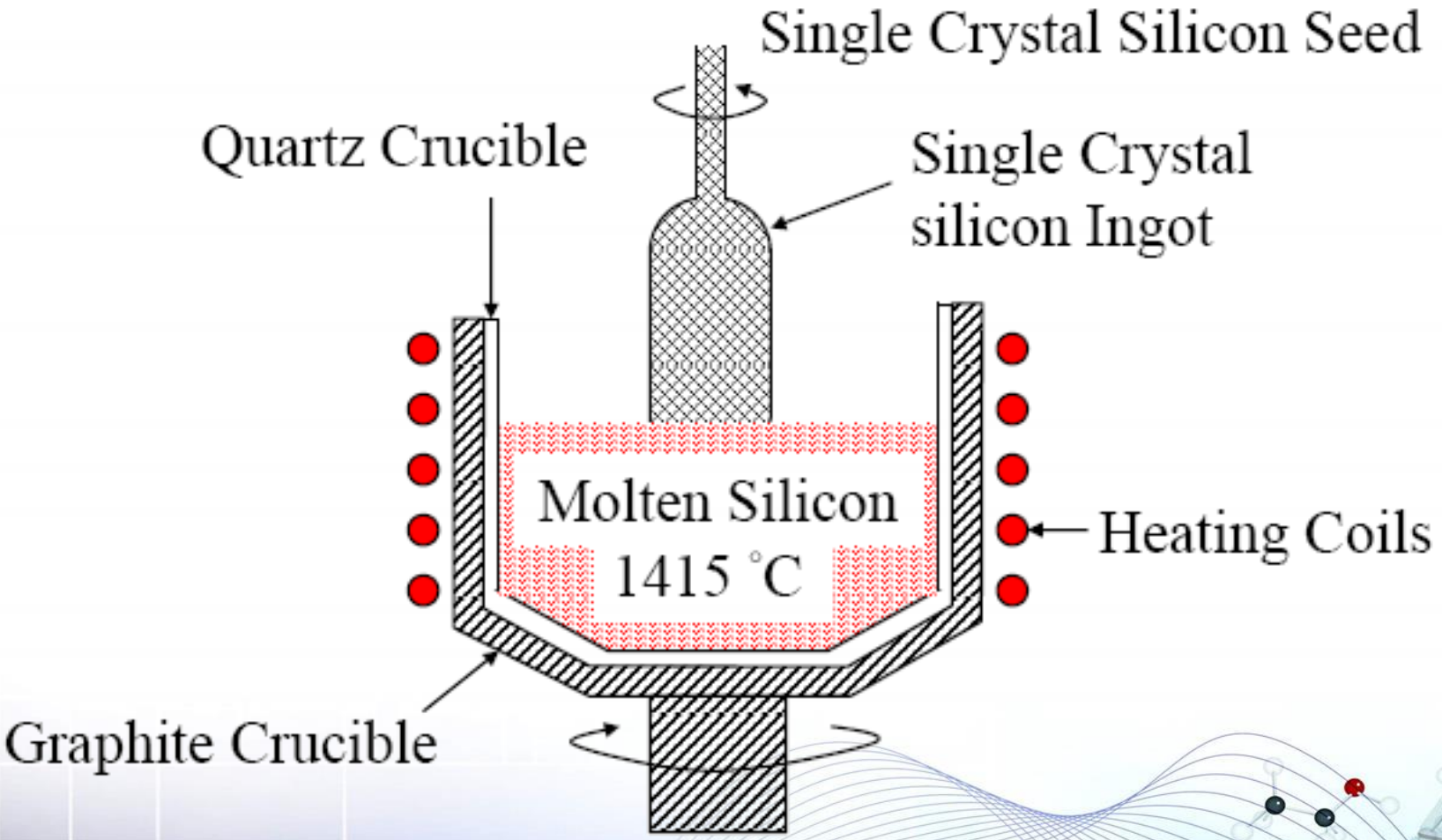


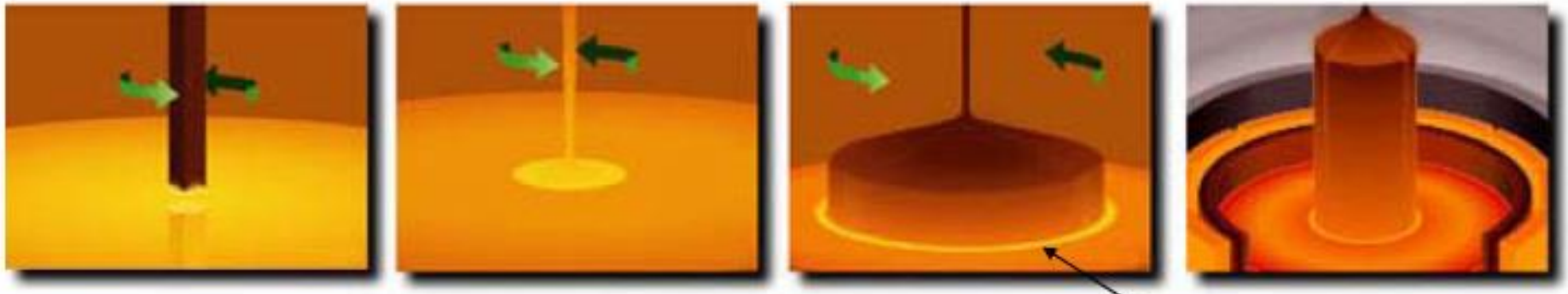
Silicon Wafers (3) — CZ (Czochralski) method

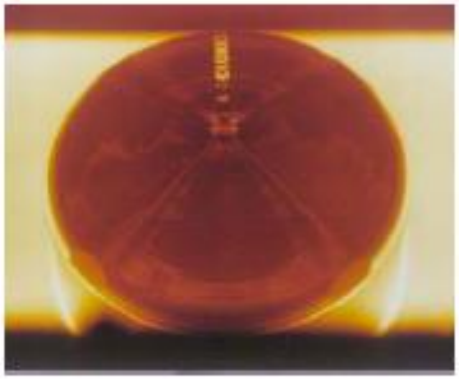


Photograph courtesy of Kayex Corp., 300 mm Si crystal puller

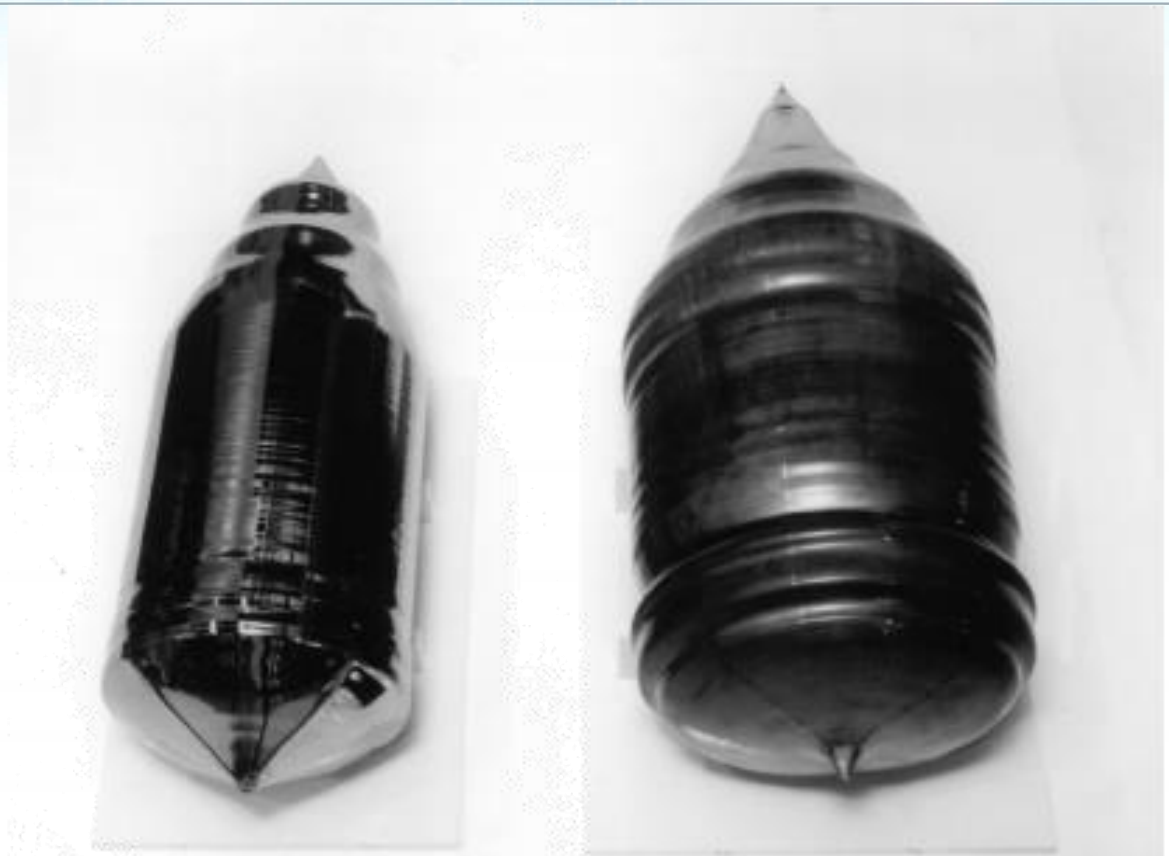
Photo 4.2

CZ Crystal Pulling



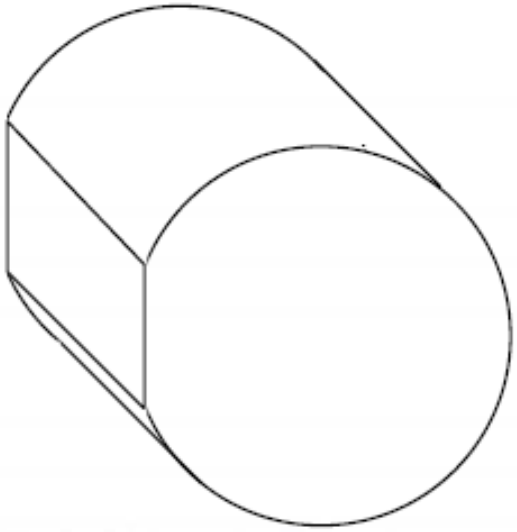


Automatic Diameter Control

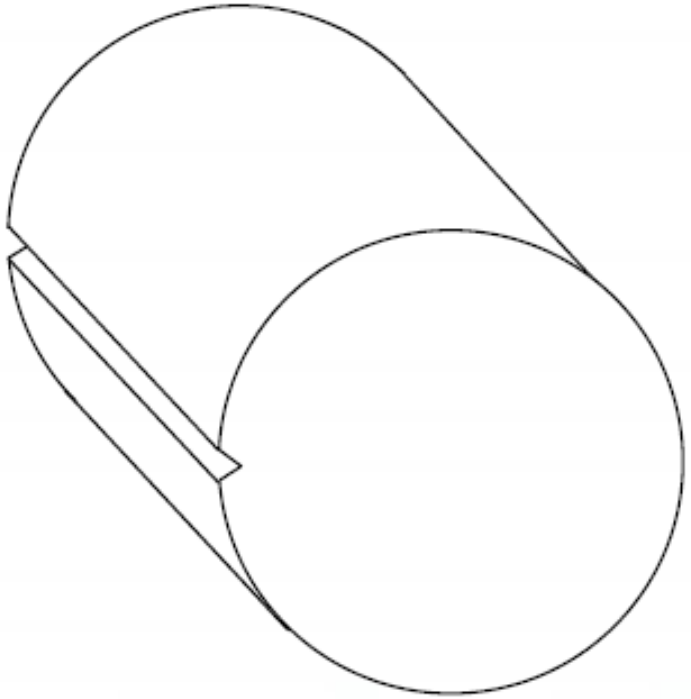


300-mm (12 in.) and 400 mm (16 in.) Czochralski-grown silicon ingots. (Photo courtesy of Sin-Etsu Handotai Co., Tokyo.)

Ingot Polishing, Flat, or Notch

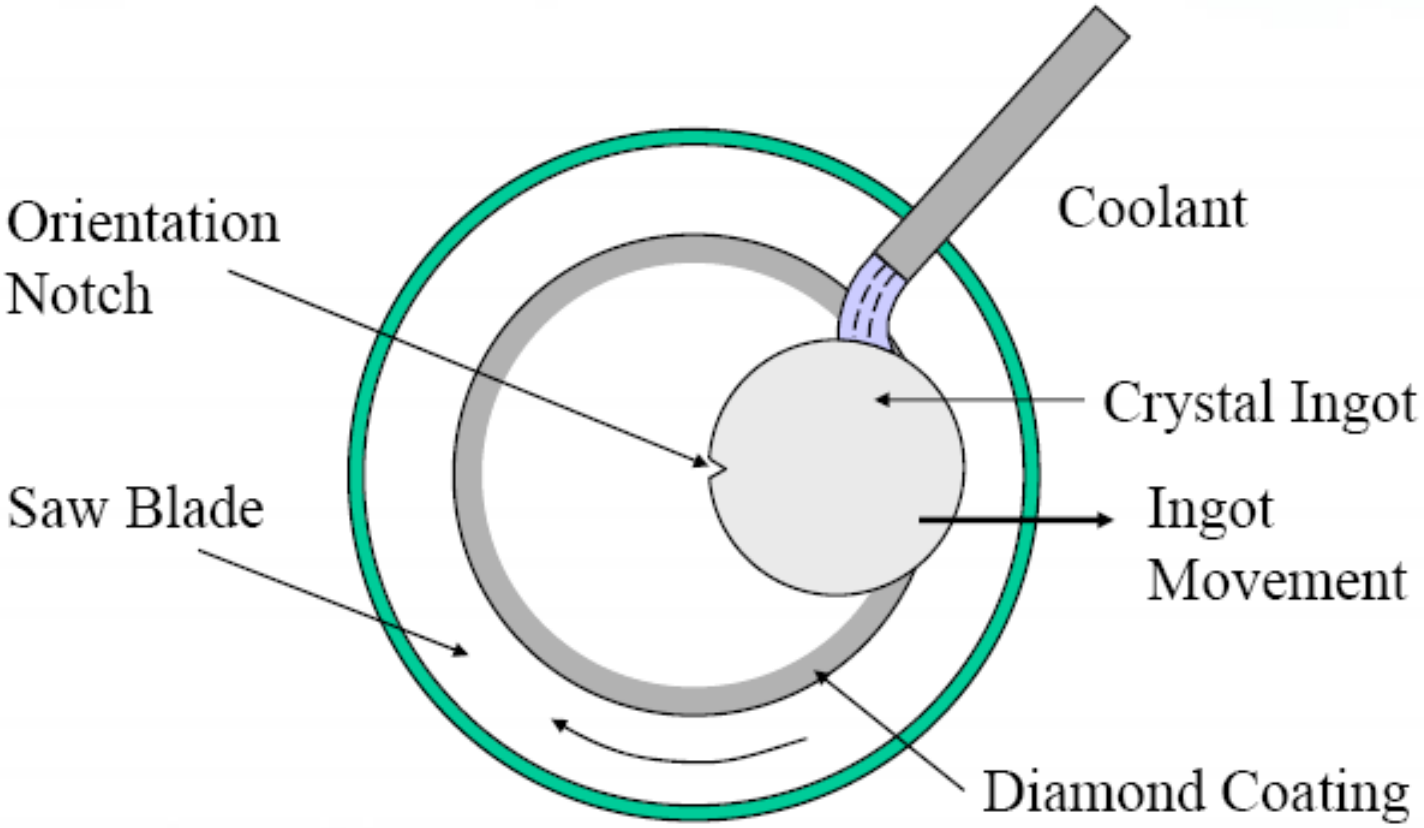


Flat, 150 mm and smaller

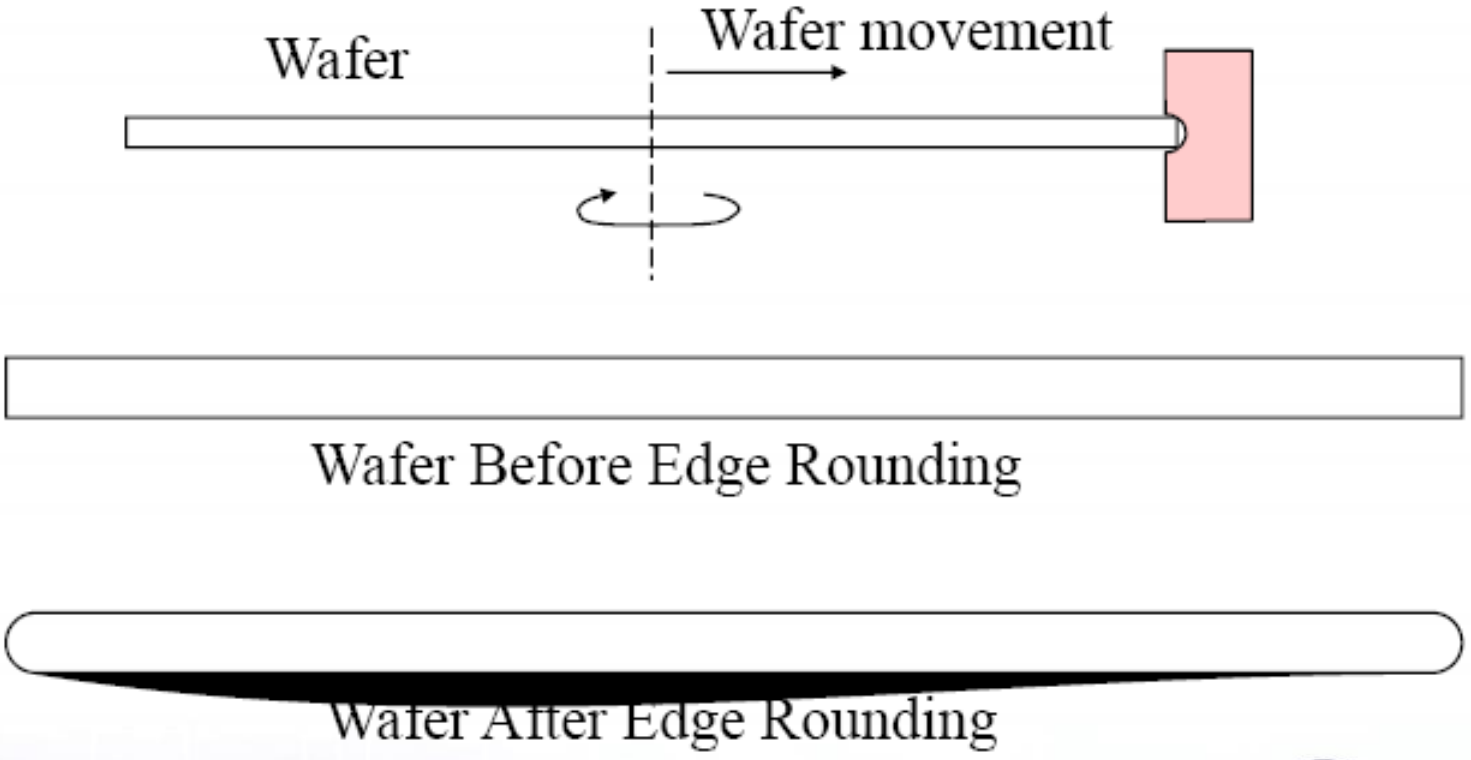


Notch, 200 mm and larger

Wafer Sawing



Wafer Edge Rounding



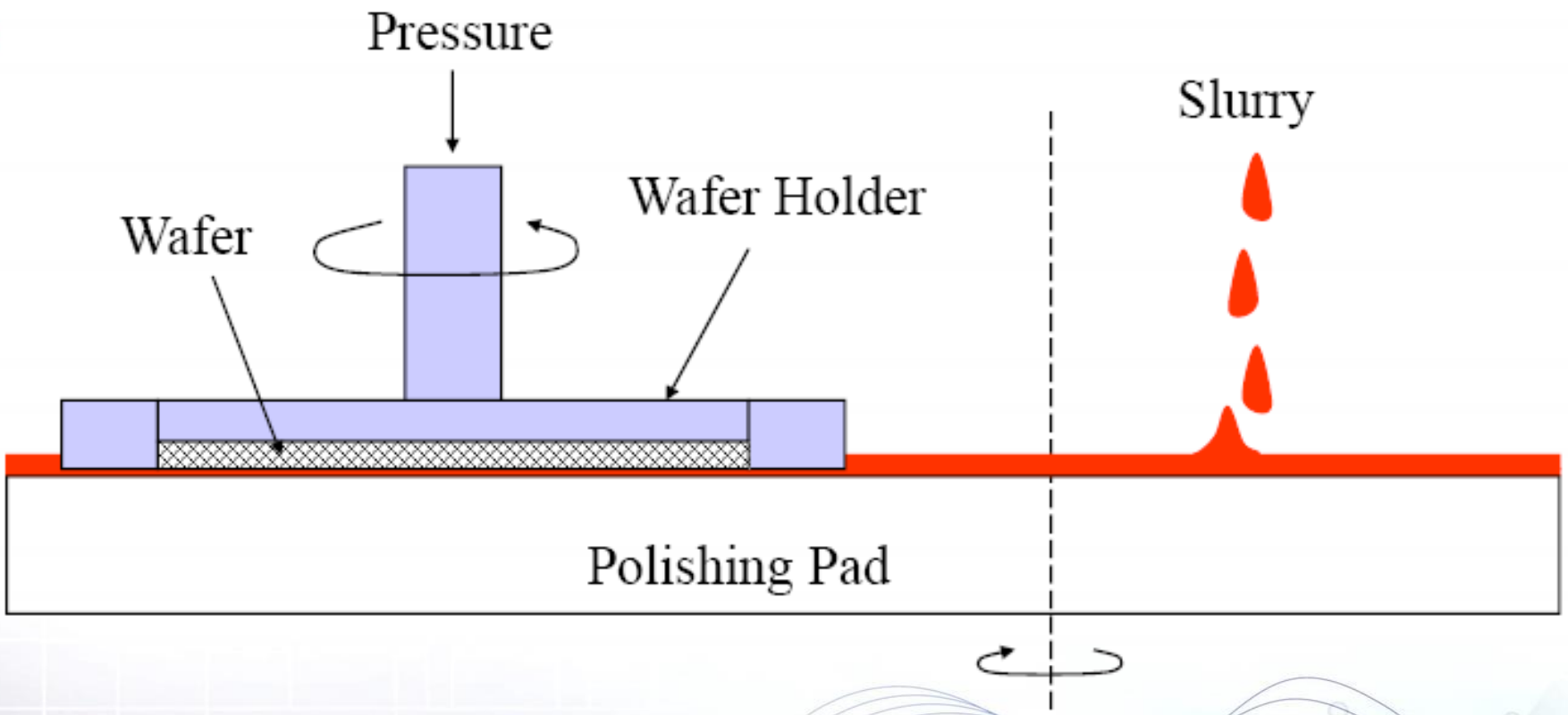
Wafer Lapping

- Rough polished
- conventional, abrasive, slurry-lapping
- To remove majority of surface damage
- To create a flat surface

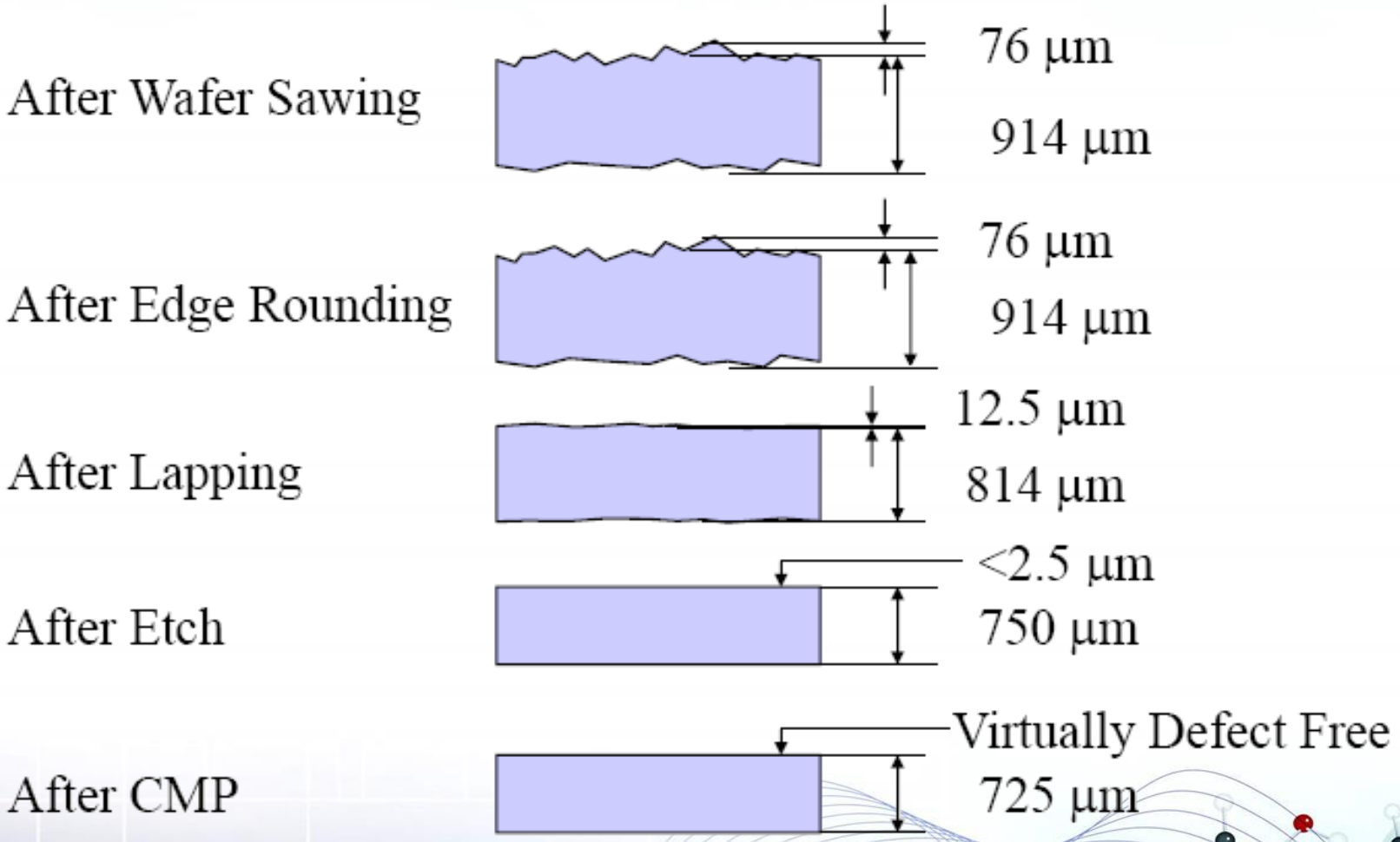
Wet Etch

- Remove defects from wafer surface
- 4:1:3 mixture of HNO_3 (79 wt% in H_2O),
- HF (49 wt% in H_2O), and pure CH_3COOH.
- Chemical reaction:
- $3\ Si + 4\ HNO_3 + 6\ HF \rightarrow 3\ H_2SiF_6 + 4\ NO + 8\ H_2O$

Chemical Mechanical Polishing

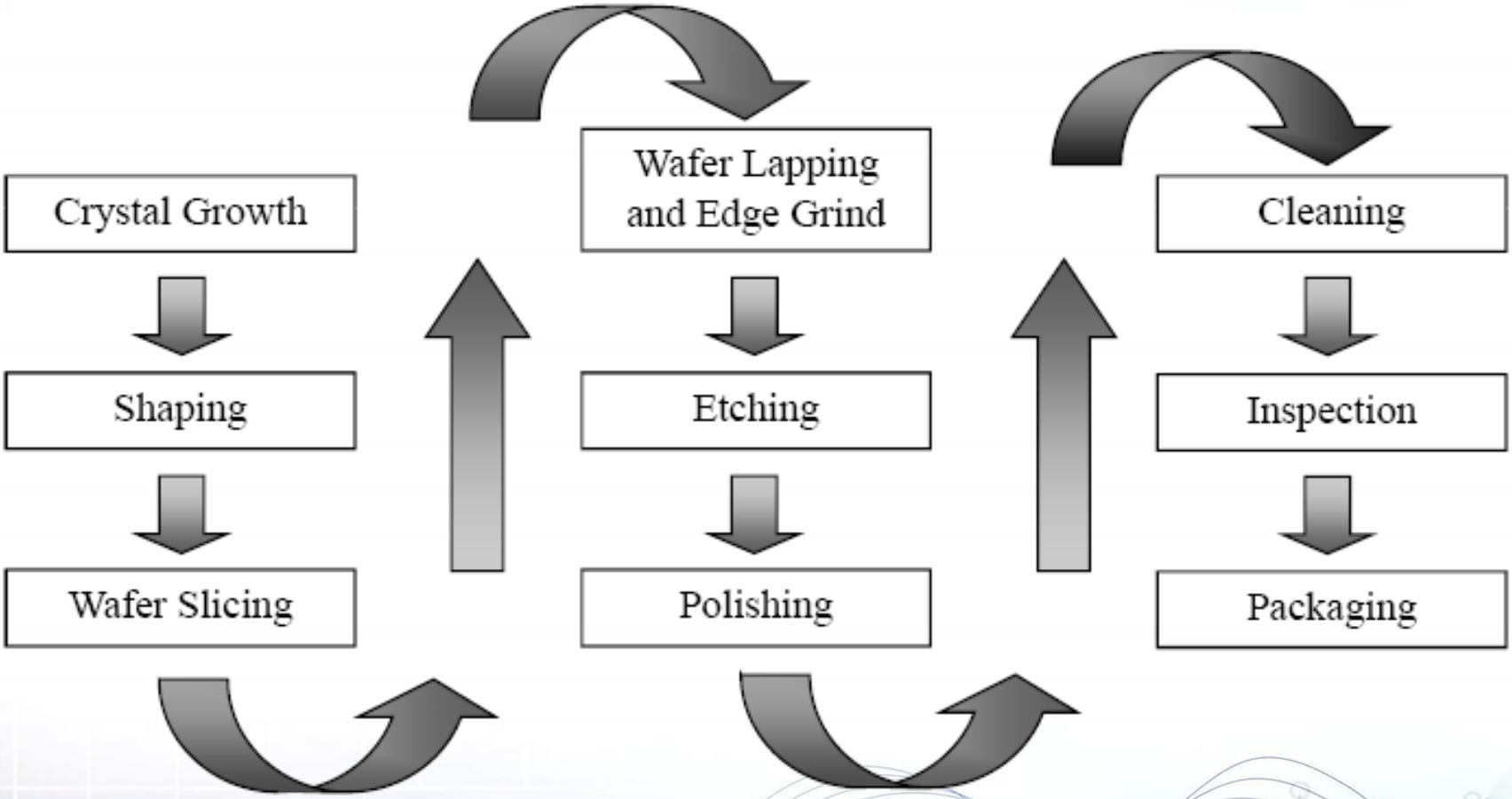


200 mm Wafer Thickness and Surface Roughness Changes

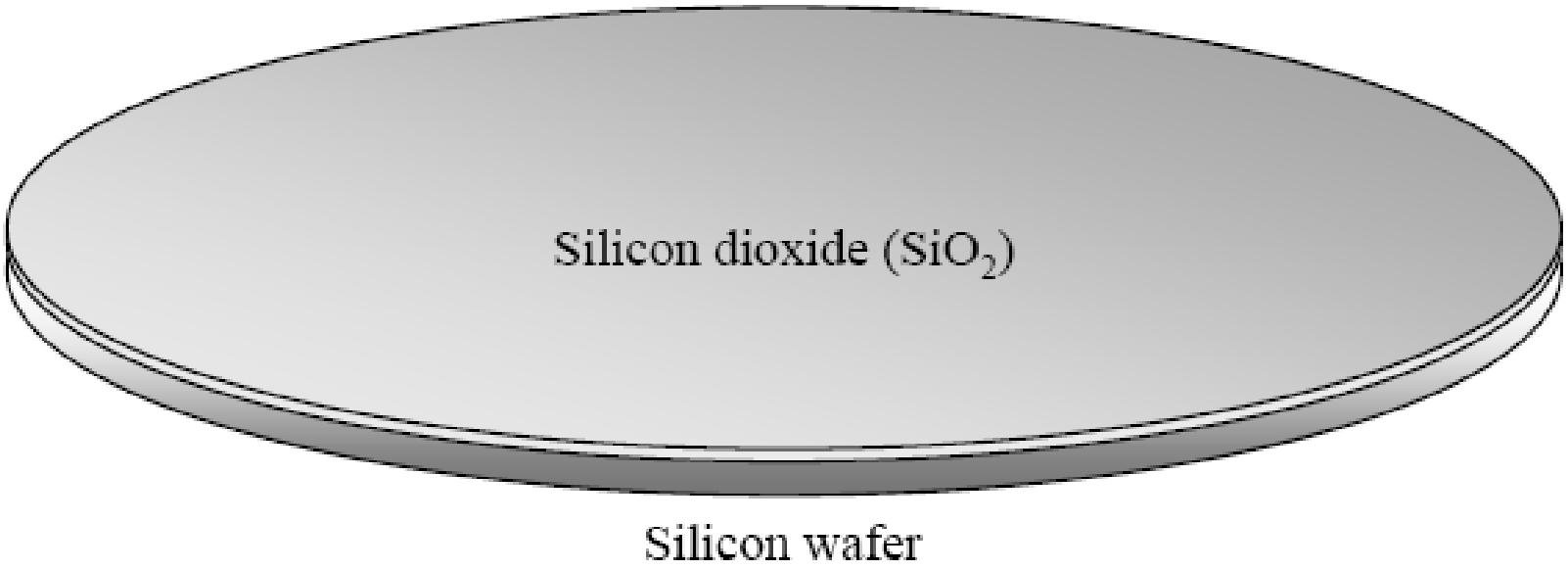


200-mm (8 in.) and 400-mm (16 in.) polished silicon wafers in cassettes.

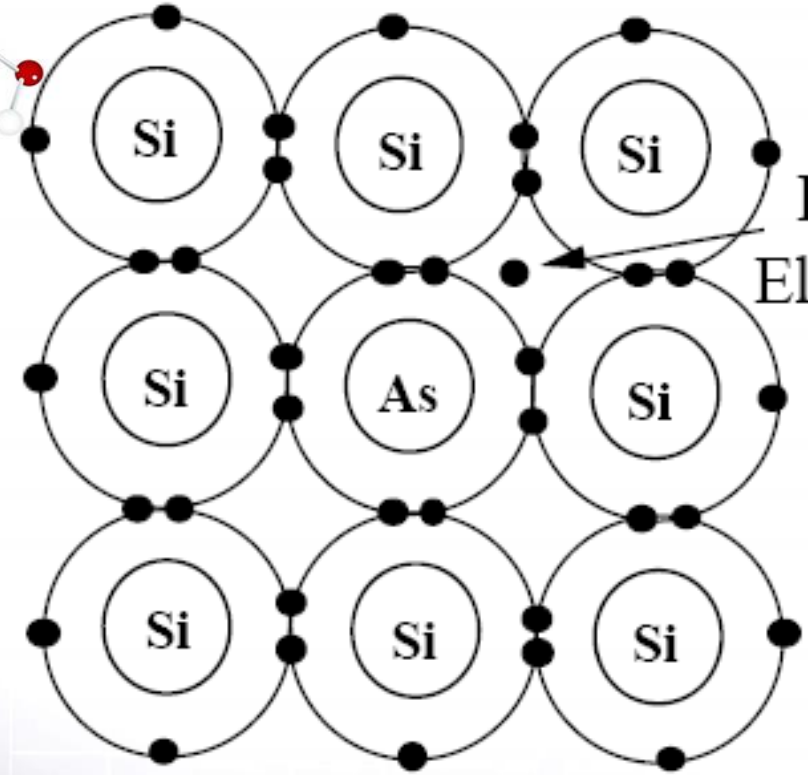
Basic Process Steps for Wafer Preparation

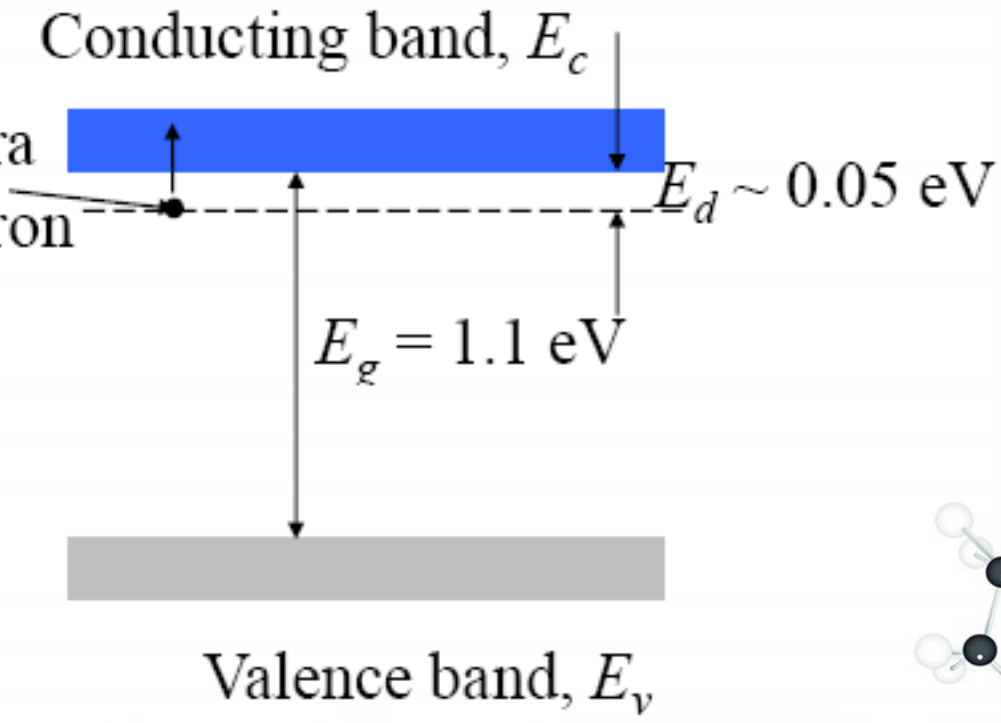


Silicon Wafers (4) — SiO_2 on Silicon Wafer

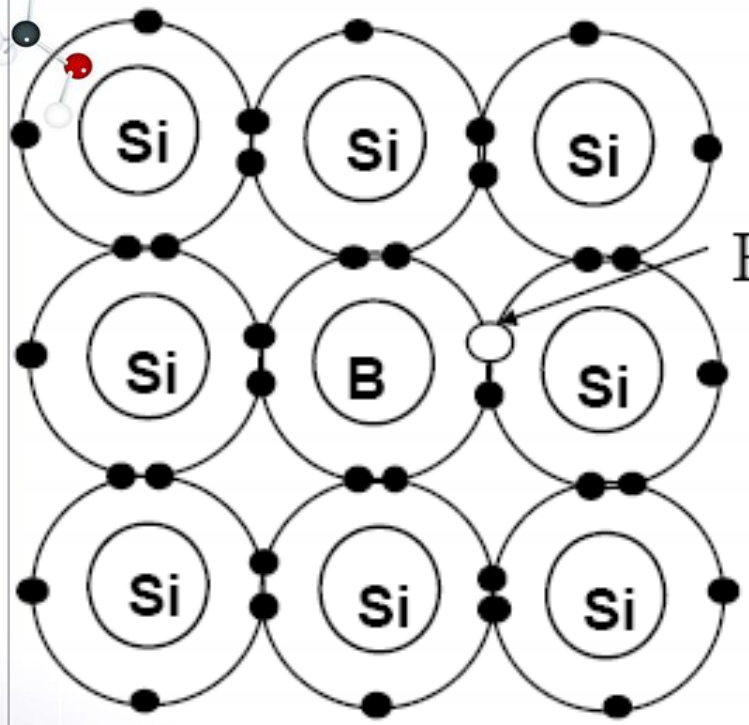


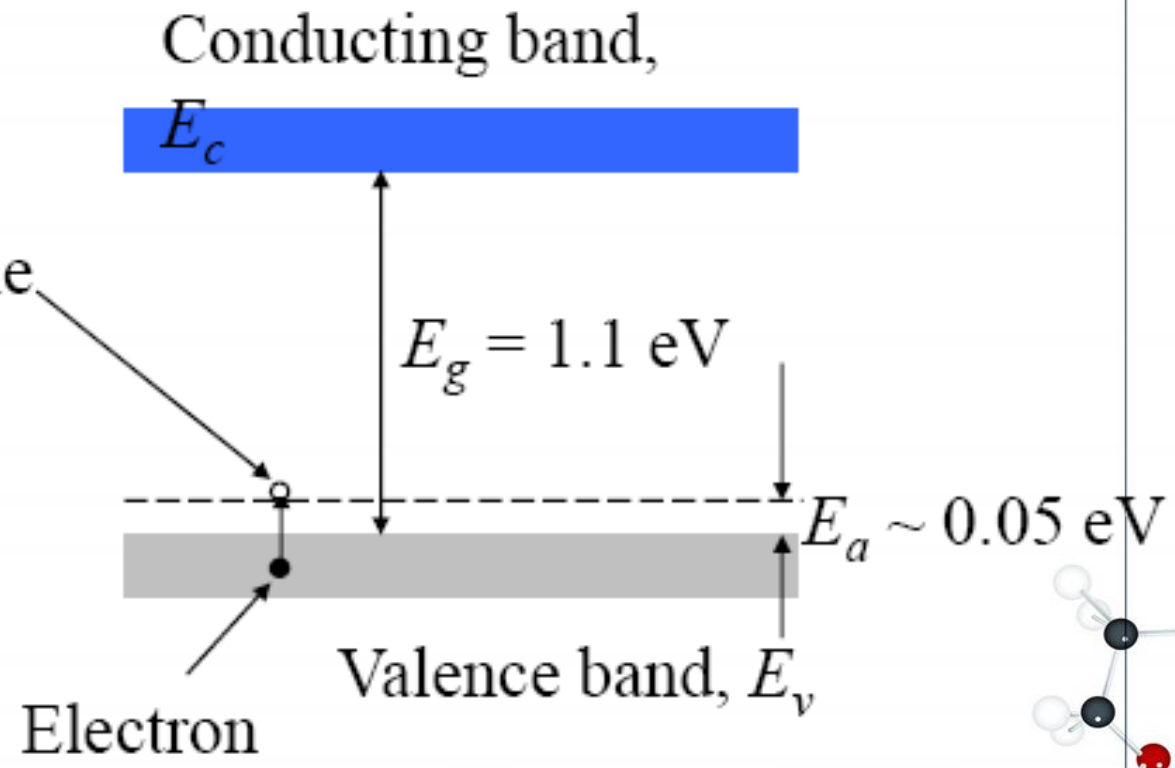
Silicon Wafers (5) — N-type Doped Silicon



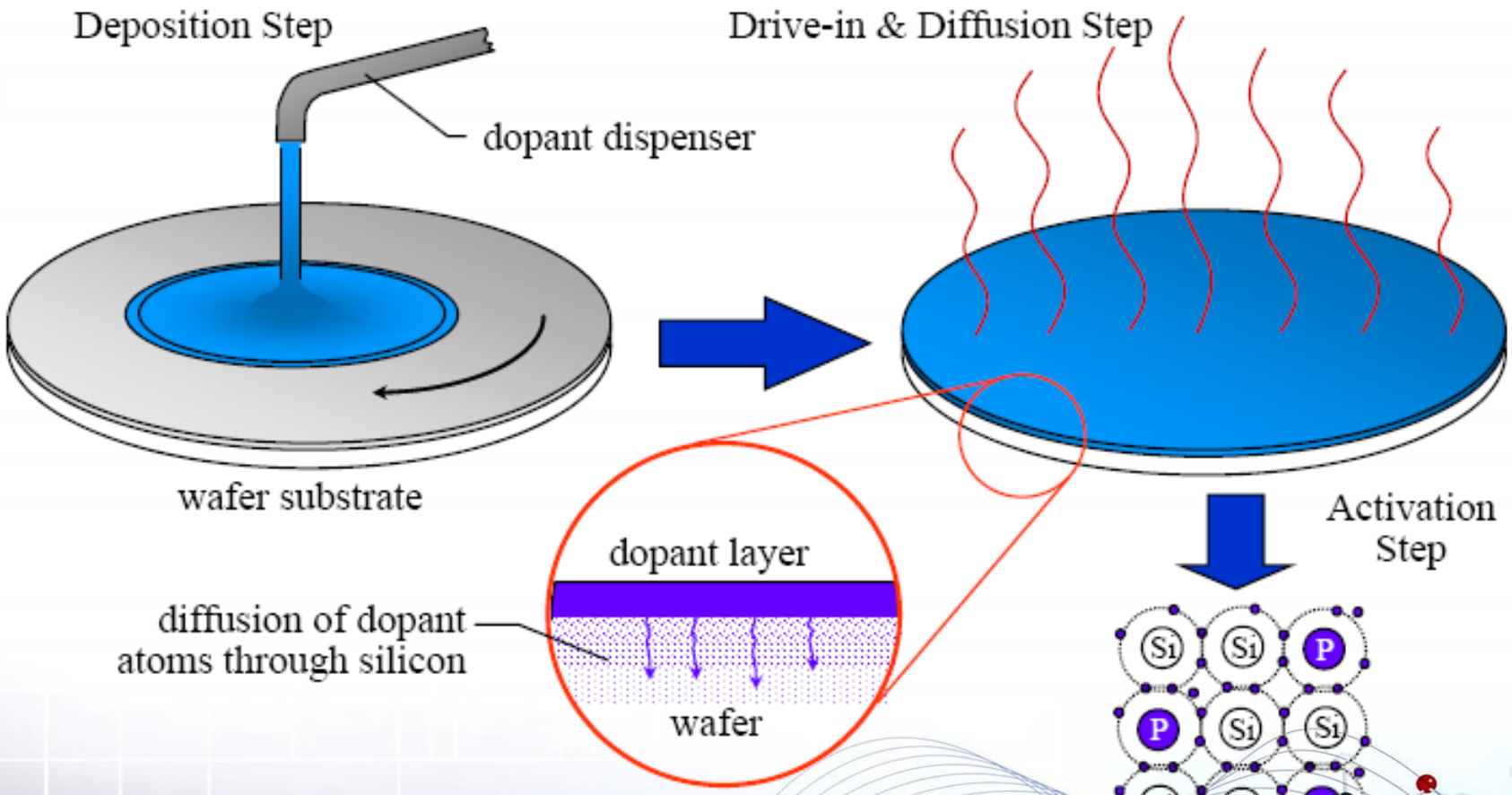


Silicon Wafers (6) — P-type Doped Silicon





Silicon Wafers (7) — Doping of Silicon



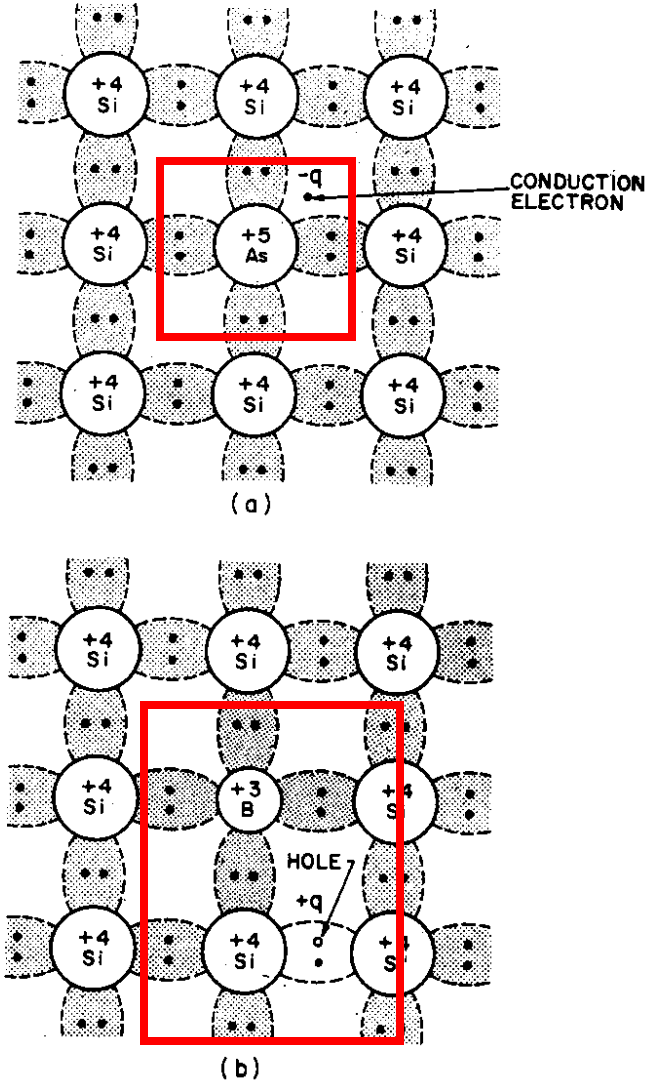
N- and P- Doped

- Increase the conductivity of the semiconductor with impurity
- N- (As, P): donate electrons
  - As^+ , P^+
  - Majority carrier : electron
  - Minority carrier : hole

負摻雜(摻入的五族元素稱為施體)

- P- (B)
  - B^-
  - Majority carrier : hole
  - Minority carrier : electron

正摻雜(摻入的三族元素稱為受體)



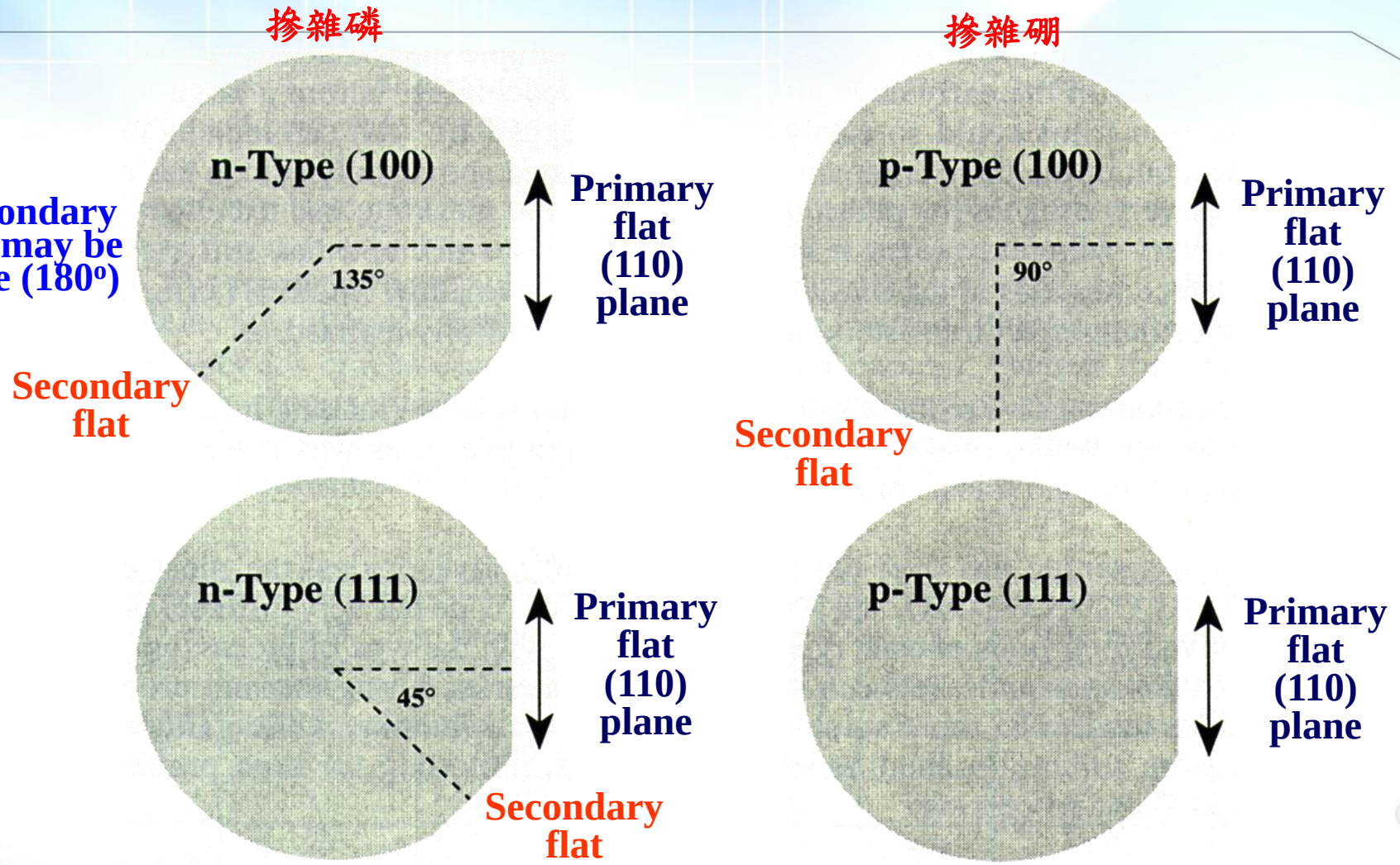


Illustration of coded "flats" as typically used on 4 in. wafer to help identify them (SEMI standard).

Silicon Wafers (8) — 矽晶圓的規格

矽晶圓規格：

4” Silicon Wafer
Type/Dopant: P/Boron P type, 摻雜硼
Orientation: (100)
Diameter: 100+/-0.5 mm
Growth Method: CZ CZ長晶方法
Thickness: 525+/-25 um
Resistivity: 20-50 ohm-cm
Particle: <=30 @ 0.3 um
Front/Back surface: polished/etched
TTV: <=10 um 晶圓最大及最小的厚度差
Bow/Warp: <=50 um 彎曲度/撓曲度
Grade: TEST 晶圓為Test等級

註：矽晶圓必須由硬殼包裝盒裝載

4" Si wafer
Type/Dopant:P/Boron
Orientation:(110)
Resistivity:1-10ohm-cm
Thickness:500-550um
Surface:Polished/Etched
Grade:Prime 晶圓為Prime等級
2 Semi-Std Flats on the (111) Plane

Photolithography

Standard RCA cleaning Process

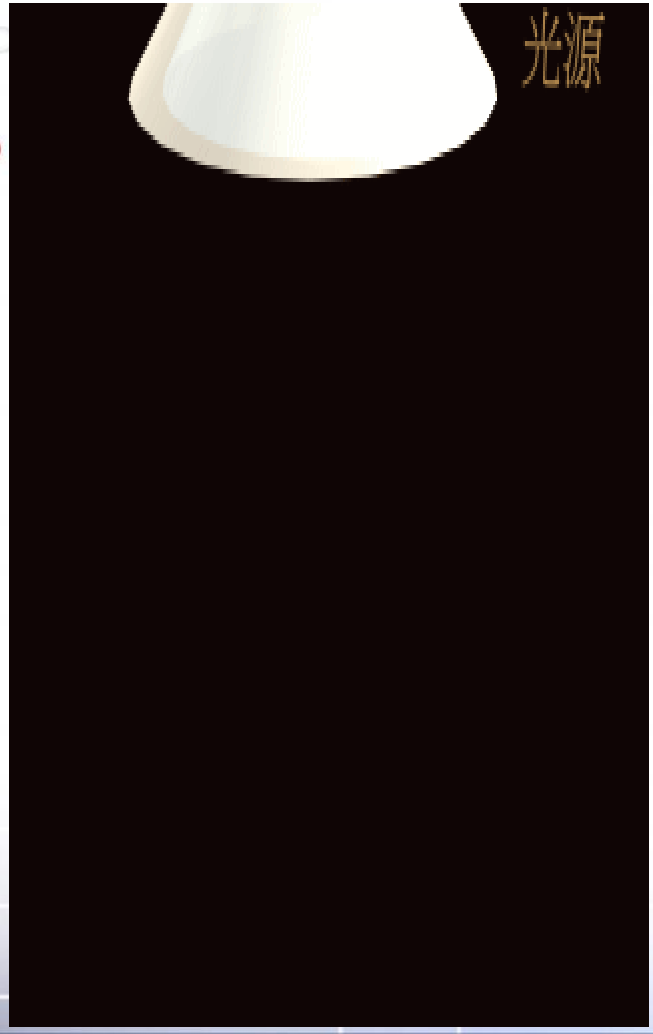
1. 沖D.I. water 5'。 比例與時間各家會有所差異
2. 去除有機物 H_2SO_4:H_2O_2=3:1 煮10'~20' (75℃~85℃)
3. 沖D.I. water 5'。
4. 去除氧化膜 HF:H_2O=1:100 10"~30"（不沾水） SiO_2會沾水 Si不沾水
5. 沖D.I. water 5'。
6. 去除微粒子與有機物 NH_4OH:H_2O_2:H_2O=0.25:1:5 煮10'~20' (75℃~85℃)
7. 沖D.I. water 5'
8. 去除金屬 HCl:H_2O_2:H_2O=1:1:6 煮10'~20' (75℃~85℃)
9. 沖D.I. water 5'
10. 去除氧化膜 HF:H_2O=1:100 10"~30"（不沾水）
11. 沖D.I. water 5'。
12. 用N_2 dry。或是旋乾(spinning dry)

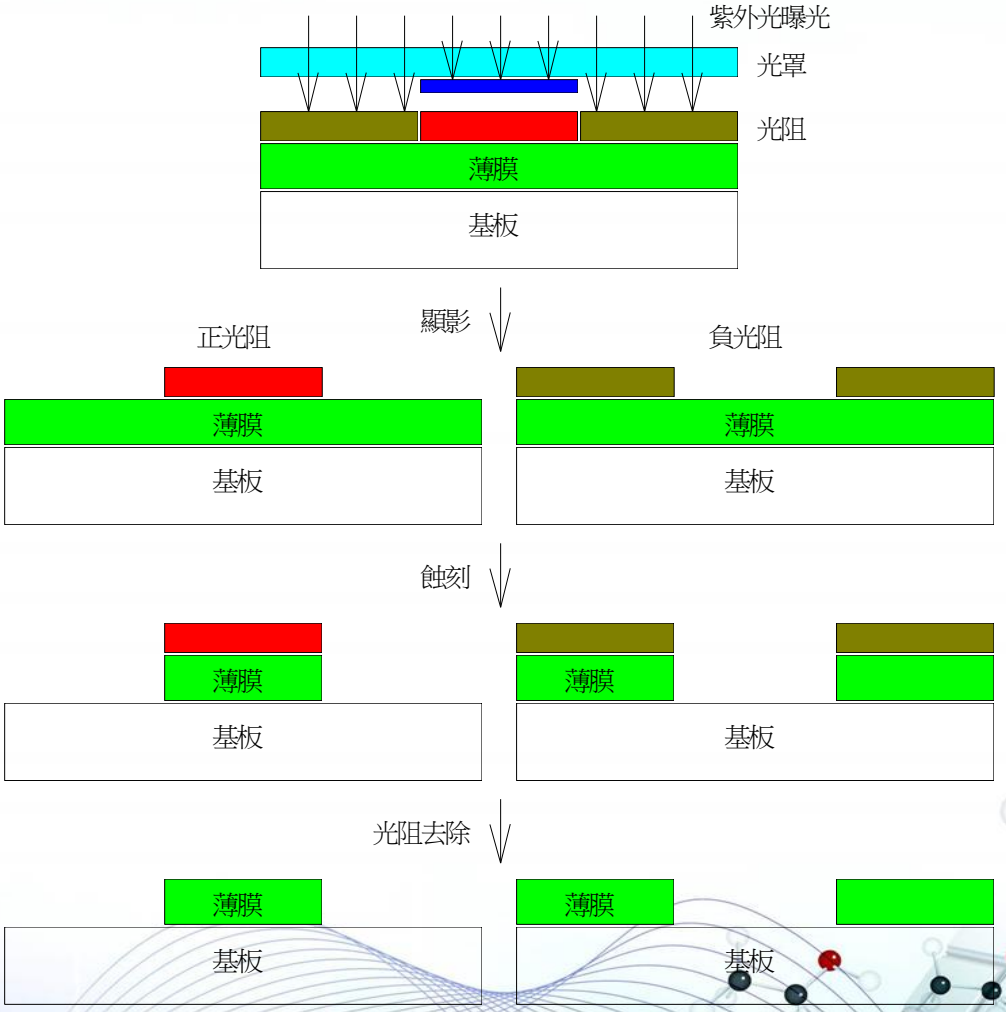
相當重要！！

※先倒入H_2O，再倒入酸或鹼，若有H_2O_2則最後倒入。

※含有HF的廢酸，請倒至HF的專用回收槽。

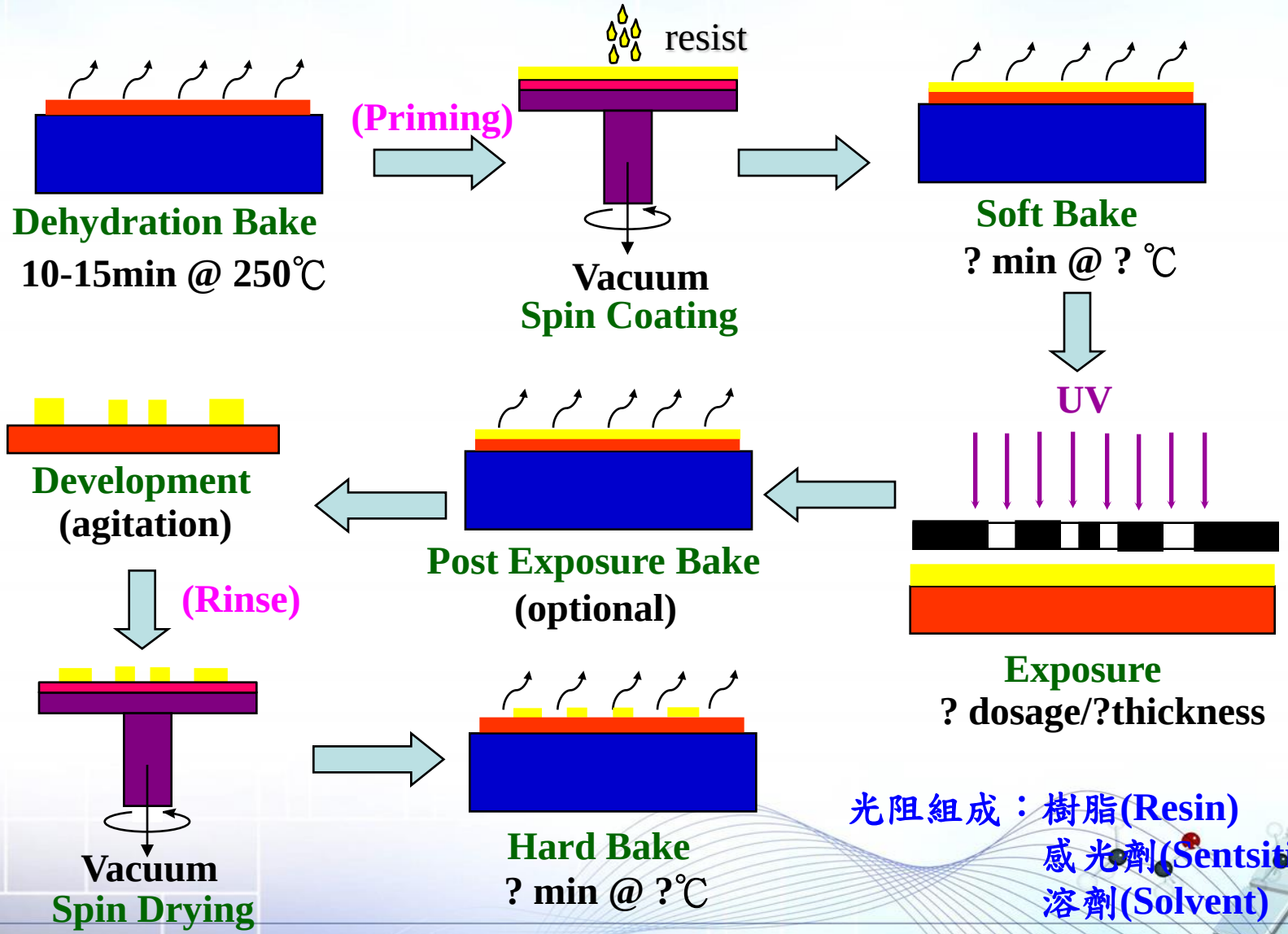
黃光微影製程(定義圖案)





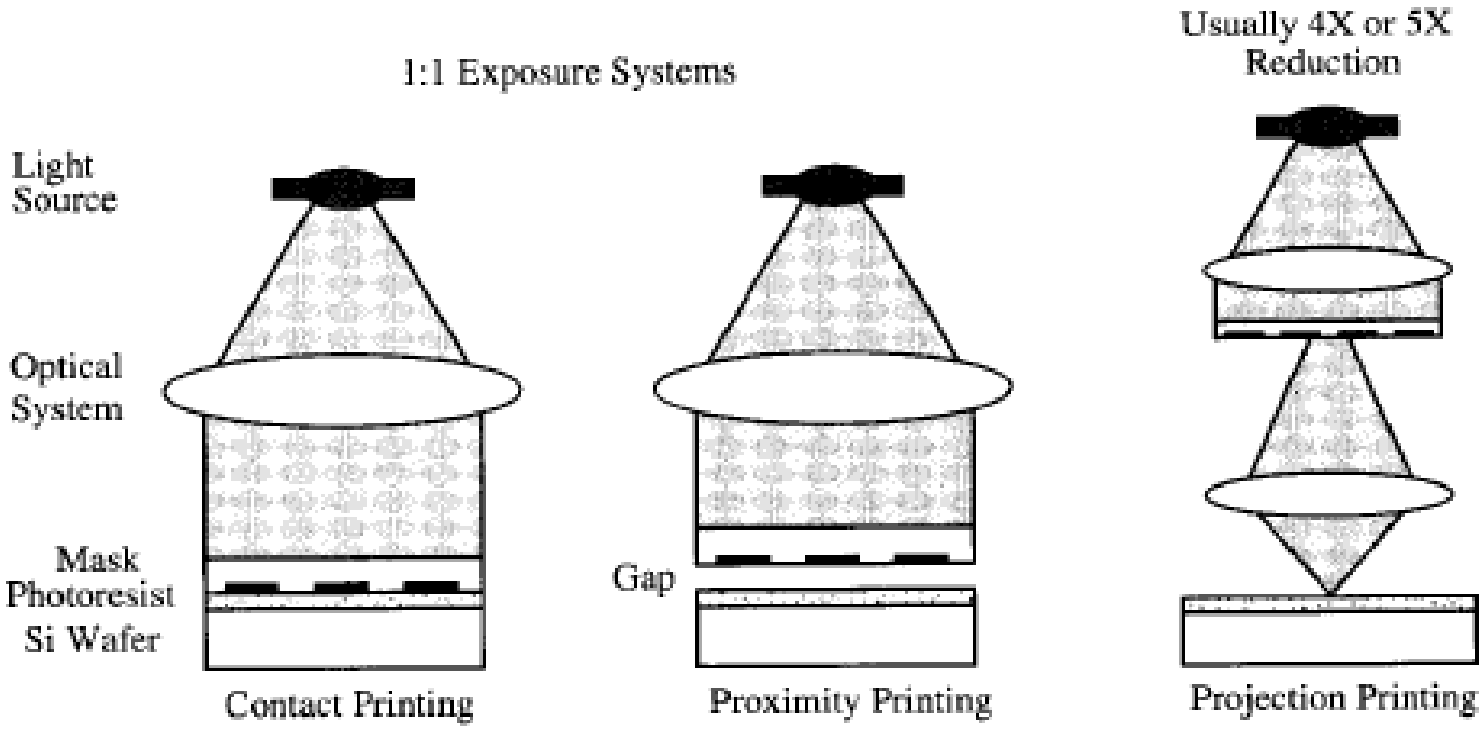
正、負光阻微影製程示意圖

光阻的微影程序

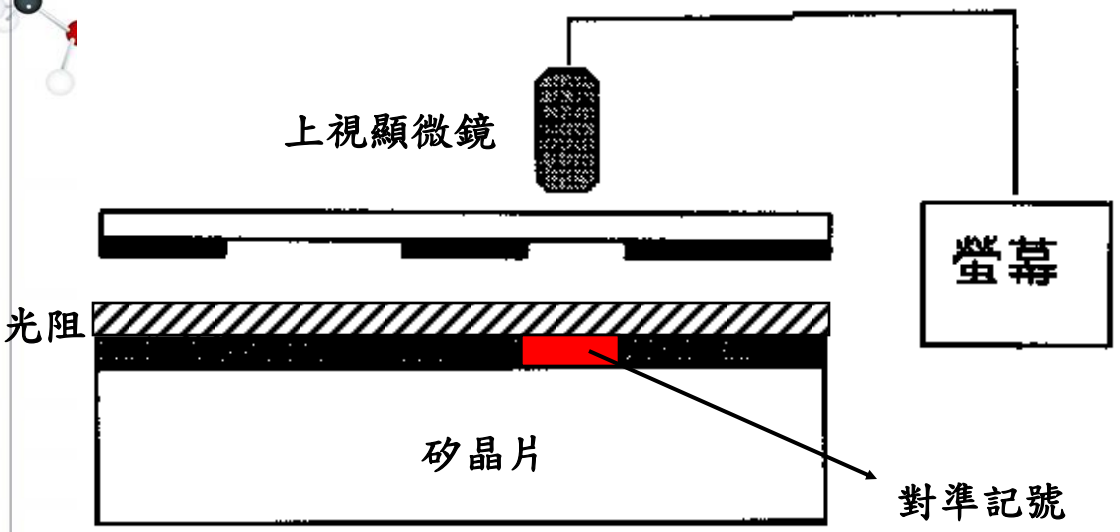


光阻組成：樹脂(Resin)
感光劑(Sentsitizer)
溶劑(Solvent)

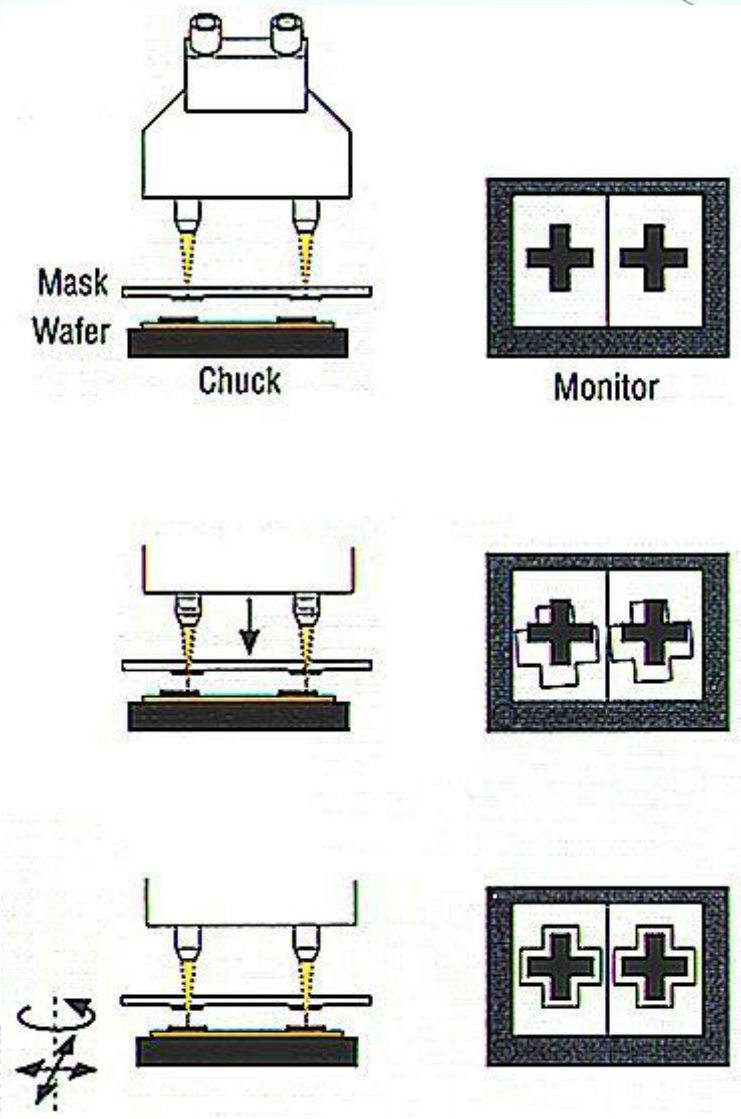
曝光(exposure)與光罩對準(mask align)



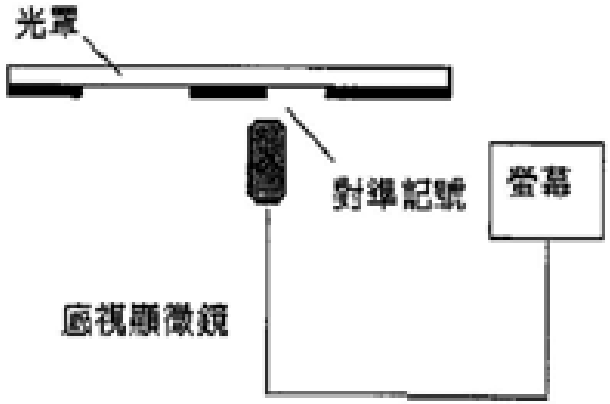
單面光罩對準

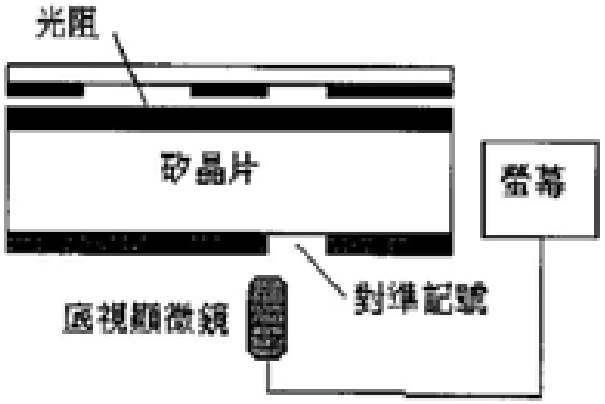


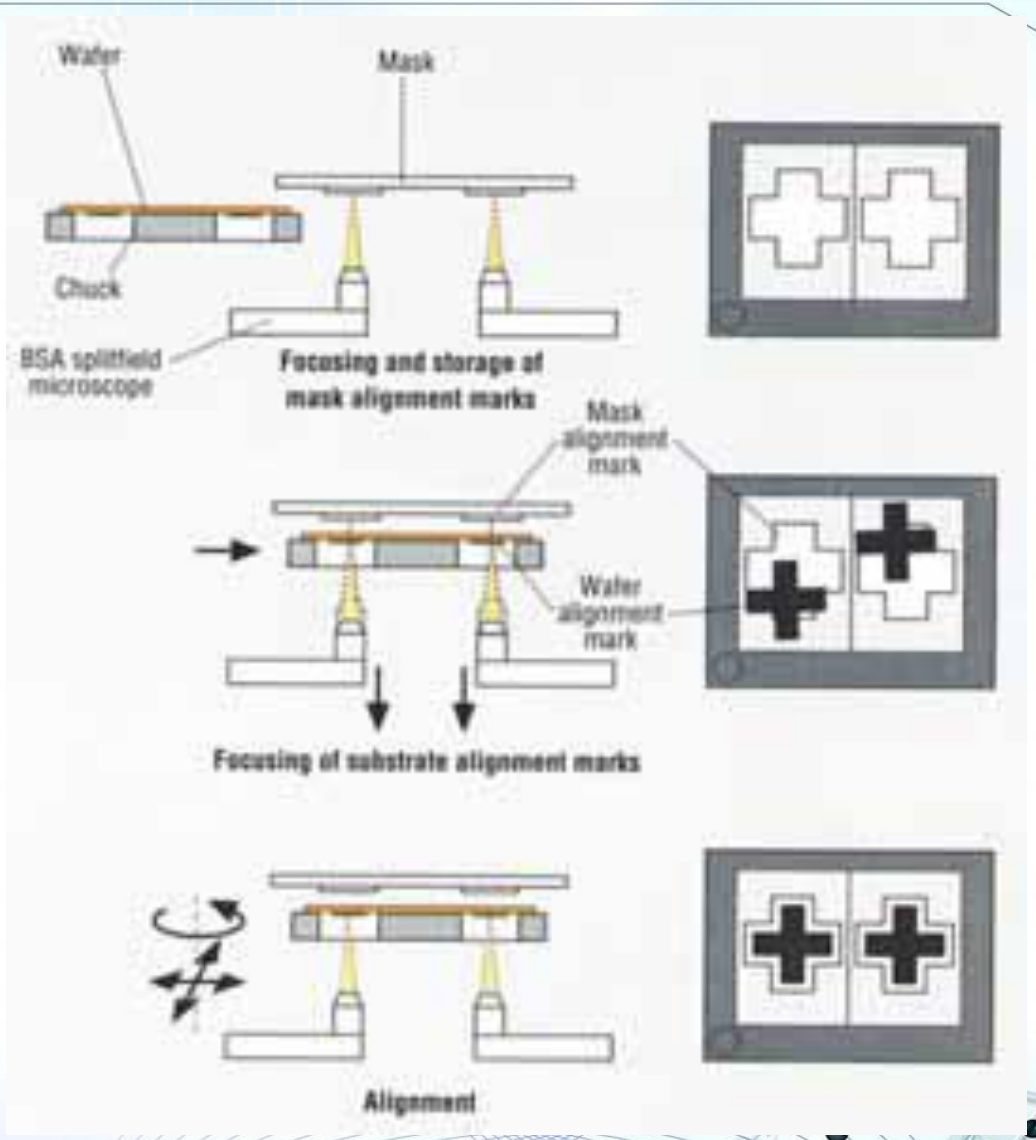
以可見光做單面對準



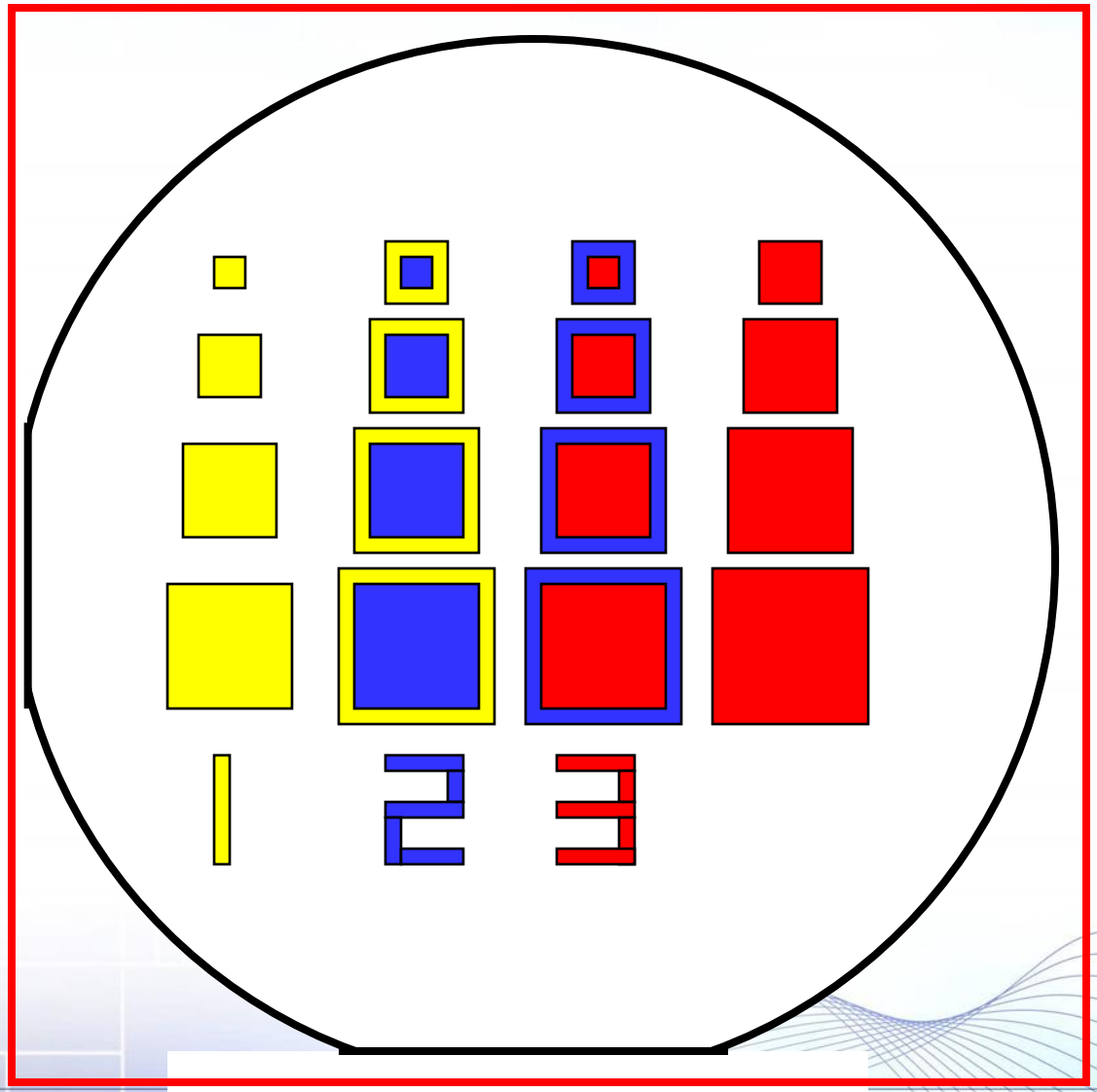
雙面光罩對準


光罩
對準記號
螢幕
區視顯微鏡


光阻
矽晶片
螢幕
對準記號
區視顯微鏡


Wafer
Mask
Chuck
BSA splitfield microscope
Focusing and storage of mask aligement marks
Mask alignment mark
Wafer alignment mark
Focusing of substrate alignment marks
Aligement

光罩-晶圓對準示意圖



Patterned Wafer

Mask 2

Mask 3

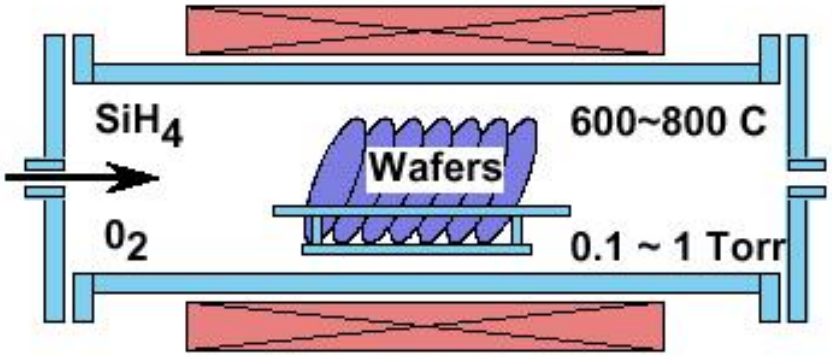
Film Vapor Deposition

真空鍍膜技術之分類

- 化學氣相沉積法(Chemical Vapor Deposition)
  - 熱CVD (Thermal CVD): LPCVD, APCVD
  - 電漿輔助CVD (Plasma-enhanced CVD)
  - 有機金屬CVD (Metal organic CVD)
- 物理氣相沉積法(Physical Vapor Deposition)
  - 濺鍍(Sputtering)
  - 蒸鍍(Evaporation)

薄膜沈積

Chemical Vapor Deposition (CVD)

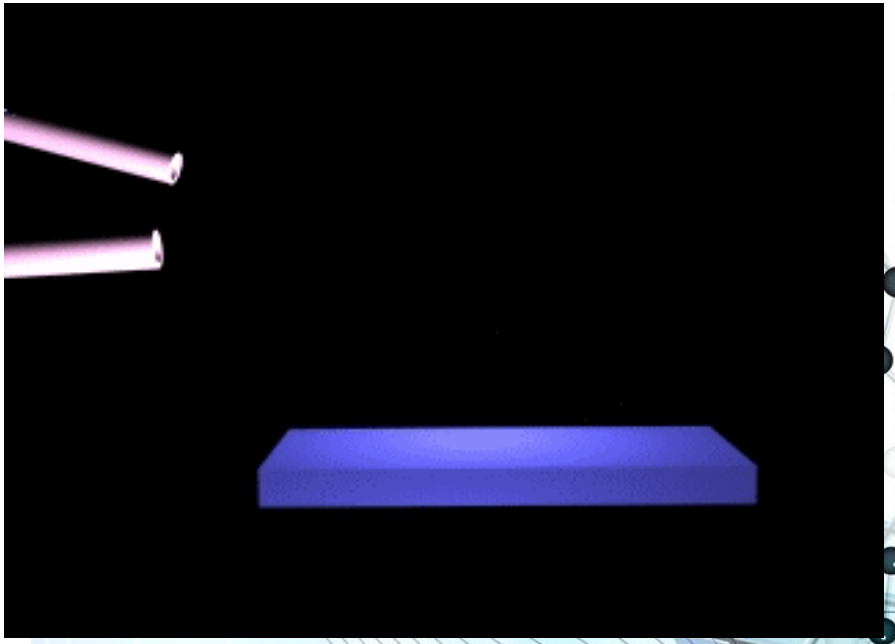


Polysilicon (~ 2 μm)
SiO2 (~ 2 μm)
PSG (~ 4 μm)
SixNy (~ 0.3 μm)
Mainly Si related materials

+ stress controllable
+ high density
- high temperature

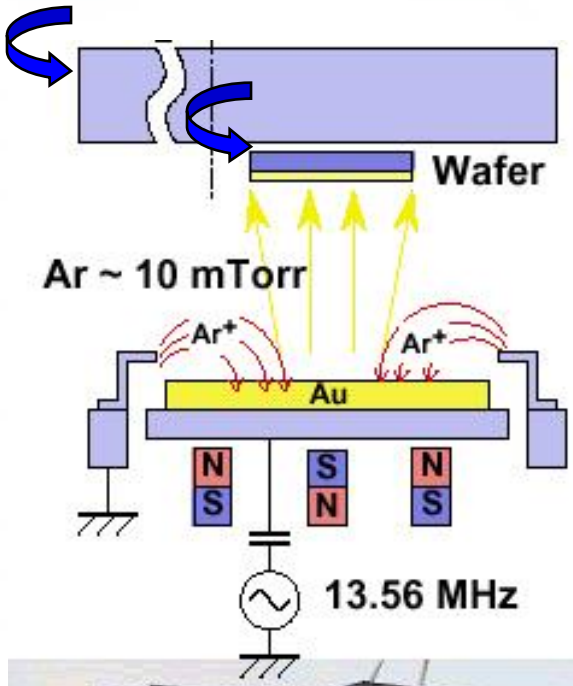
- **PECVD**
- **LPCVD**
- **APCVD**
- **MOCVD**

(光電薄膜沈積)



Physical Vapor Deposition (PVD)

Sputtering



Metal (Cr, Au, Ni, Fe, Ti, Cu, Pt, ...)

Alloy (FeNi, TiNi, ...)

Oxide (SiO_2, Al_2O_3, ...)

Nitride (AlN, SiN, ...)

All in 0.1 ~ 5μm range

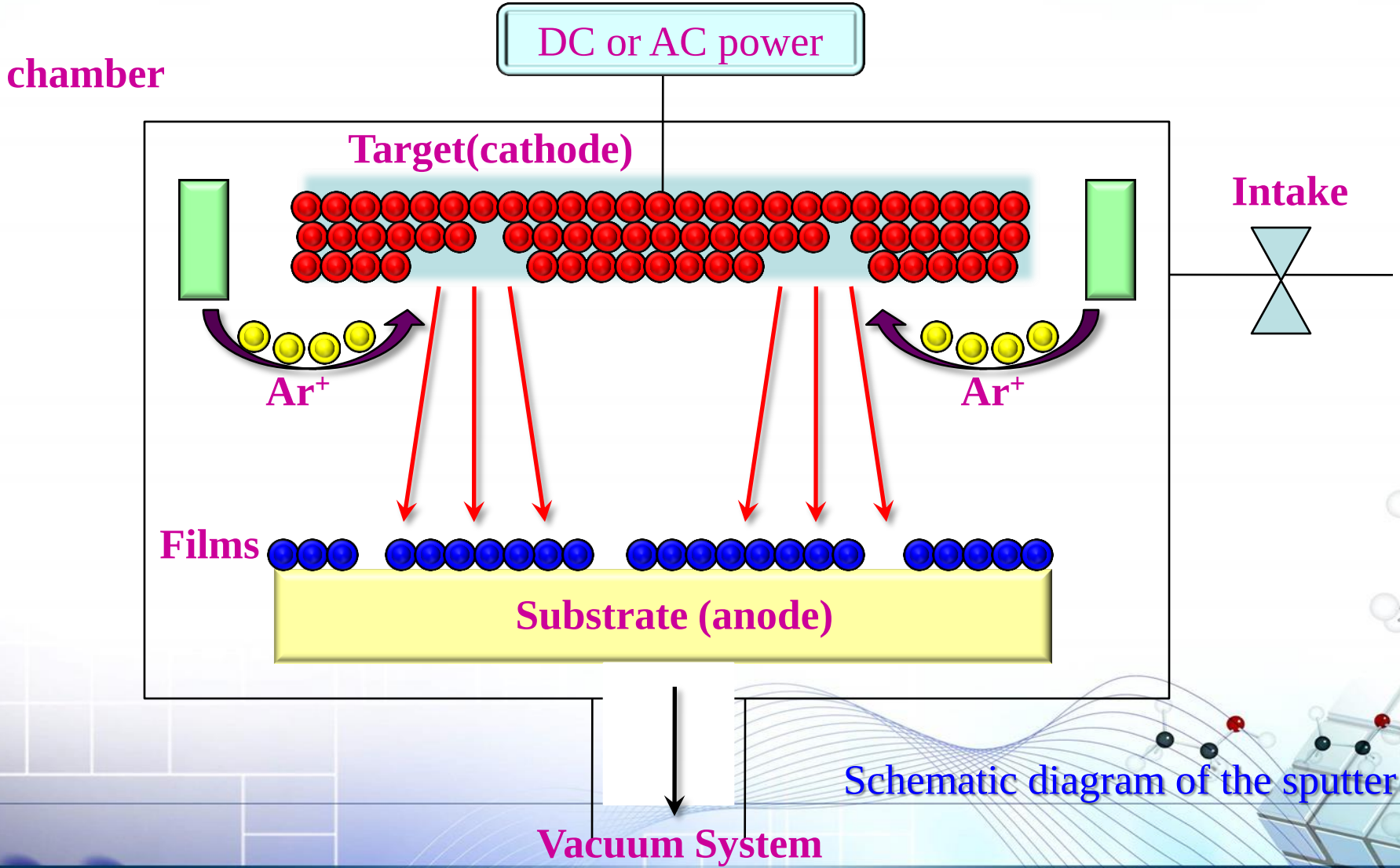
TiN, TiW

+ various materials other than oxide or nitride

- residual stress

- less density

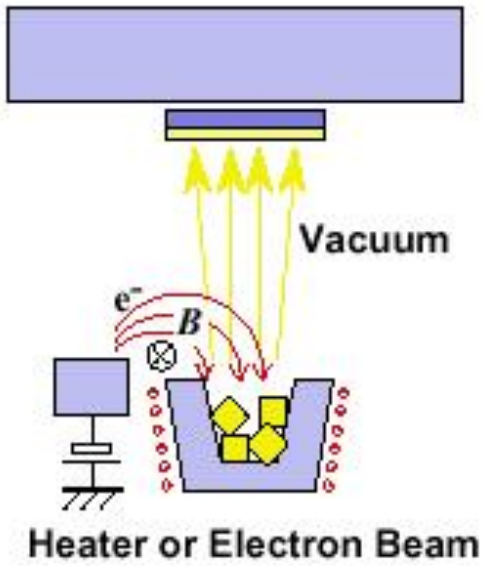
Sputtering Process



Schematic diagram of the sputter

Evaporation (PVD)

(Joule heat or Electron beam)



Metal (Cr, Au, Ni, Fe, Ti, Cu, Pt, ...)

Alloy (FeNi, TiNi, SiW, ...)

Oxide (MgO, ...)

Nitride (AlN, SiN, ...)

All in 0.1 ~ 5μm range

蒸鍍對合金或是化合物的沈積成份控制性差

+ high melting temp. materials

+ density higher than sputtering (EB)

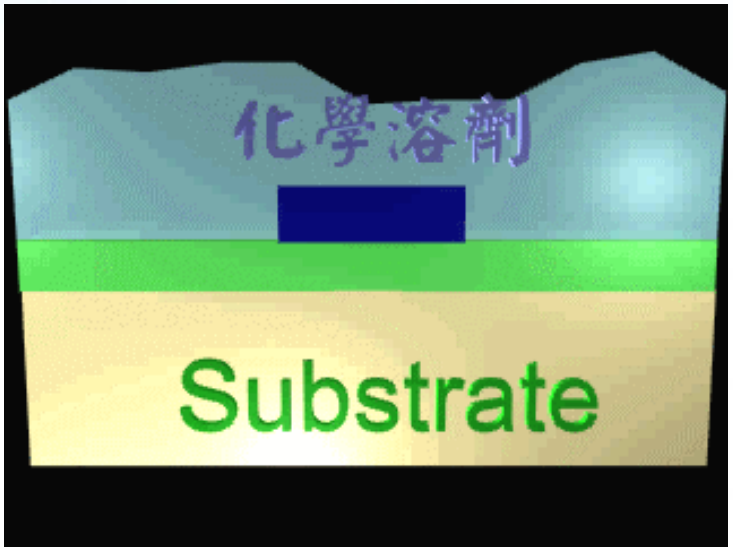
- poor adhesion (JH)

Dual E-gun evaporator

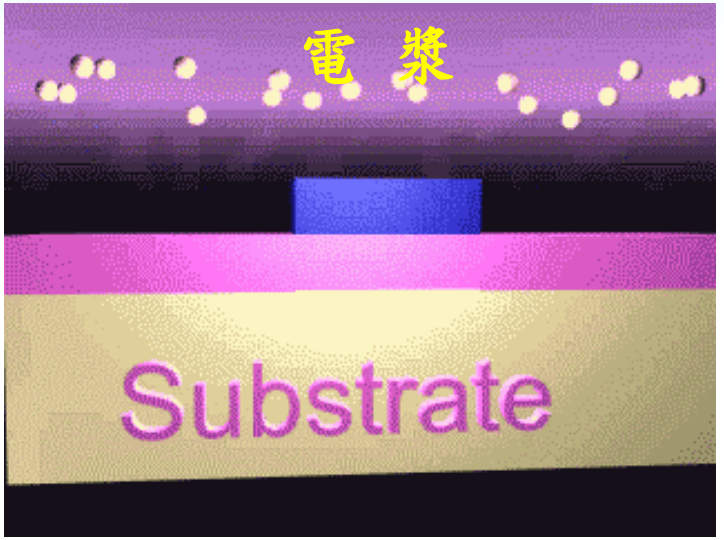
(交大半導體技術中心)

Silicon Etching Technique

溼式與乾式蝕刻



濕式蝕刻法

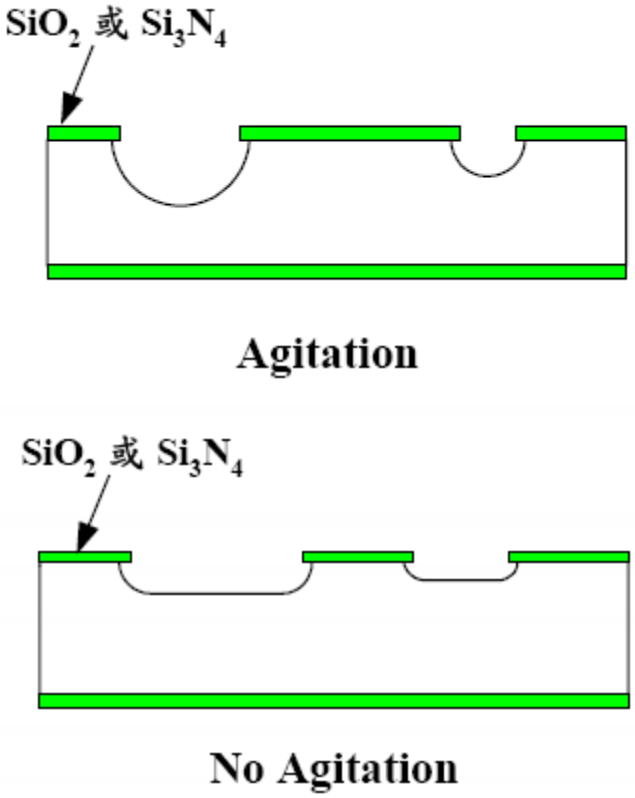


乾式蝕刻法

矽濕式蝕刻技術

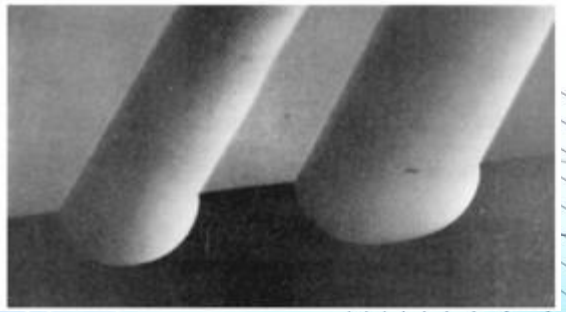
Silicon Wet Etching Technique

Wet Etch (1) — Isotropic Etching of Silicon

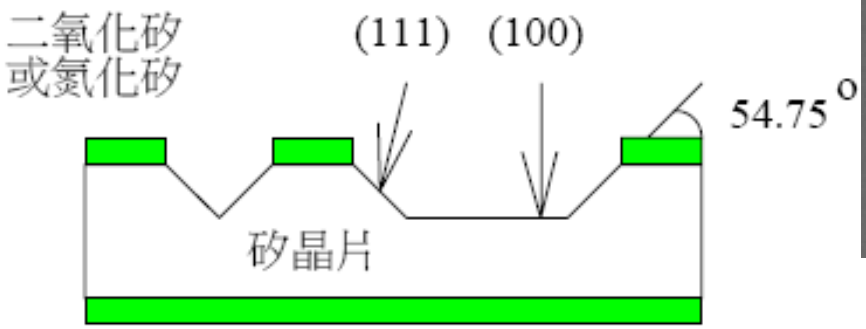


Effects of mask geometry and agitation for isotropic wet etching

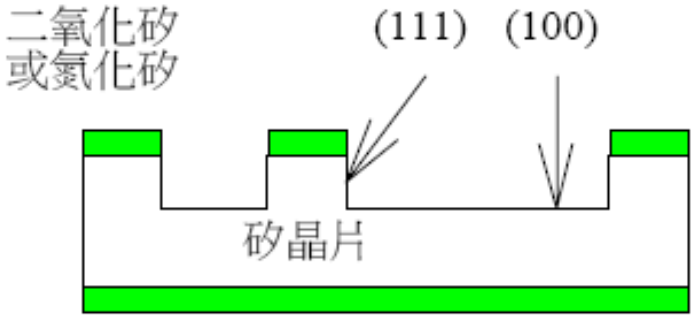
- **Etchant:**
  HNA (HF, HNO3, CH3COOH)
- **Room temperature (<50℃)**
- **Diffusion control**
- **High etching rate (50μm/min)**
- **Undercut mask**
- **Mask:**
  Au/Cr or Si3N4 is good
  SiO2 is simple
- **Undercut嚴重**
- **Dimension定義嚴重失真**



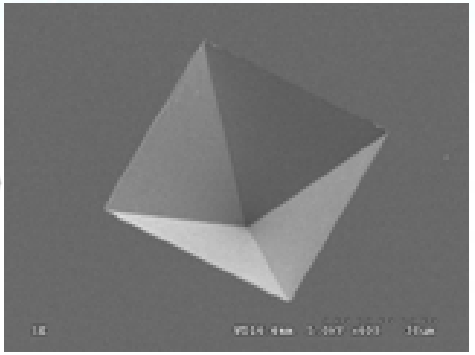
Wet Etch (2) — Anisotropic Etching of Silicon

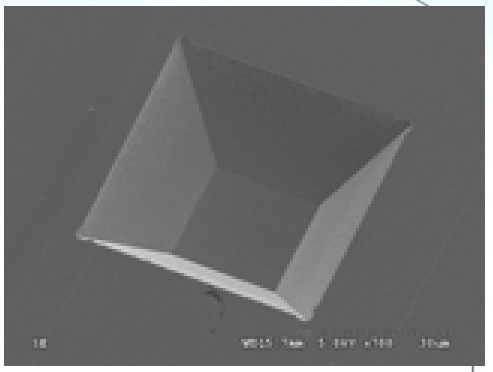


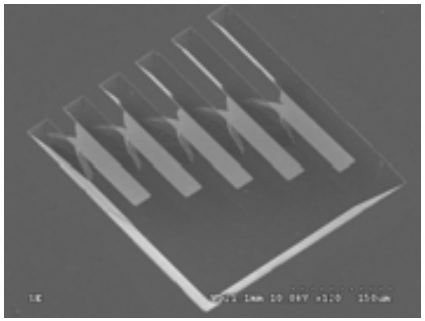
(a) <100>矽晶片



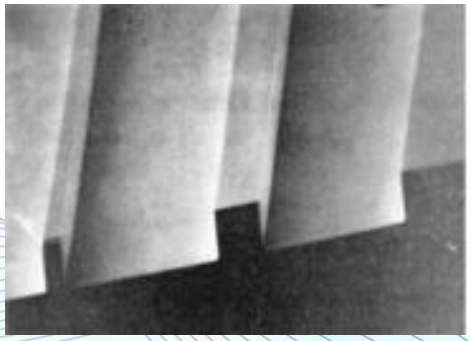
(b) <110>矽晶片







(100)



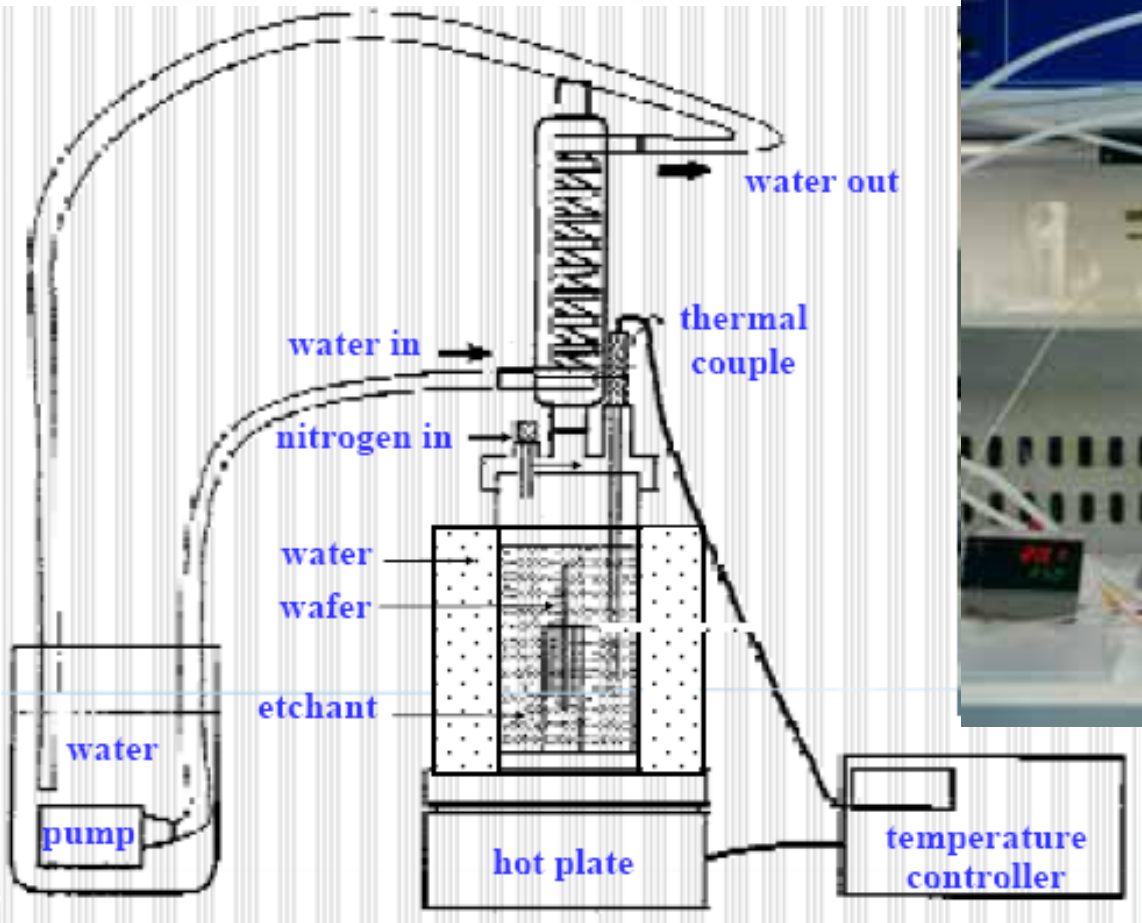
(110)

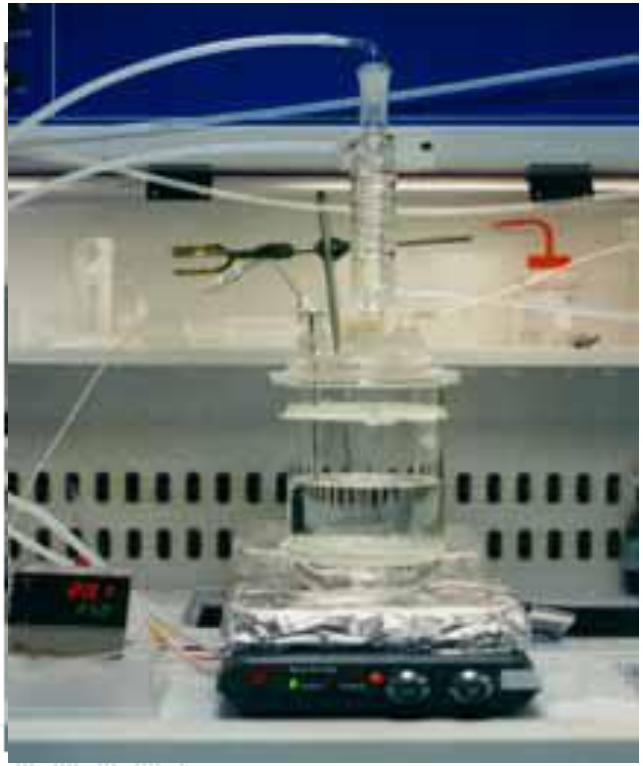
- **Etchant:**
  KOH, TMAH, EDP, H2N4

Wet Etch (3) — 蝕刻液組成與蝕刻特性

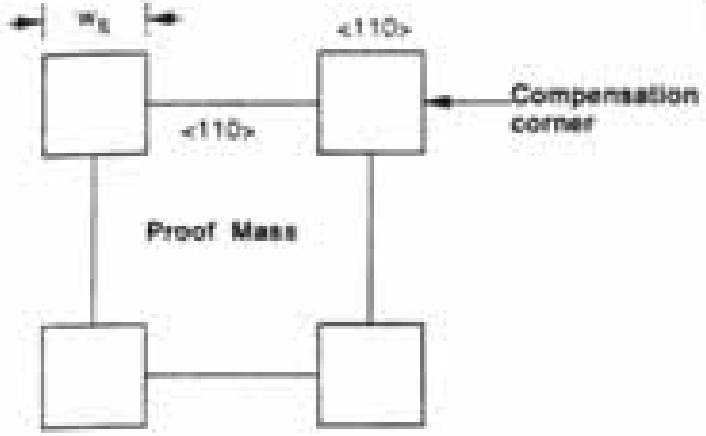
蝕刻液	組成	溫度 (°C)	蝕刻率 (μm/min)	(100)/(111) 蝕刻率比值	摻雜硼蝕刻率 降低倍數	蝕刻幕罩與 蝕刻率(nm/min)
KOH (water)	44 g 100 ml	85	1.4	400:1	$\geq 10^{20}$ cm^{-3} 降低20倍	二氧化矽(1.4) 氮化矽
KOH (isopropyl)	50 g 100 ml	50	1.0	400:1		
ethylenediamine pyrocatechol (water)	750 ml 120 g 100 ml	115	0.75	35:1	$\geq 7\times10^{19}$ cm^{-3} 降低50倍	二氧化矽(0.2) 氮化矽,金,鉻, 銀,,銅,鉭
ethylenediamine pyrocatechol (water)	750 ml 120 g 240 ml	115	1.25	35:1		
TMAH (water)	25 %	80	0.4	*	$\geq 2.5\times10^{20}$ cm^{-3} 降低40倍	二氧化矽
H_2N_4 (water, isopropyl)	100 ml 100 ml	100	2.0	*	無相關性	二氧化矽,鋁
NaOH (water)	10 g 100 ml	65	0.25-1.0	*	$\geq 3\times10^{20}$ cm^{-3} 降低10倍	二氧化矽(0.7) 氮化矽

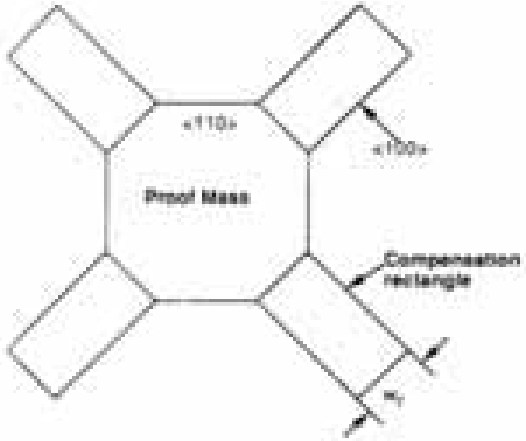
Wet Etch (4) — Etching apparatus

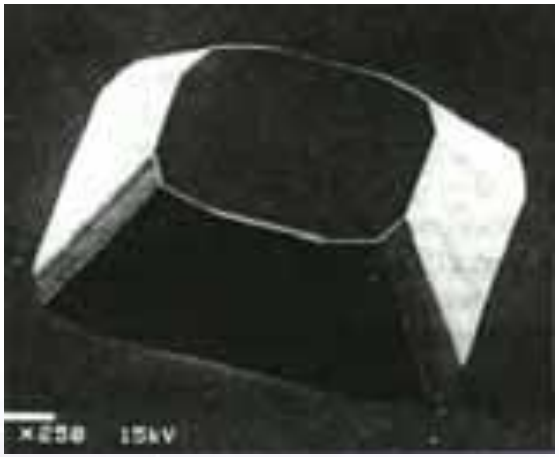


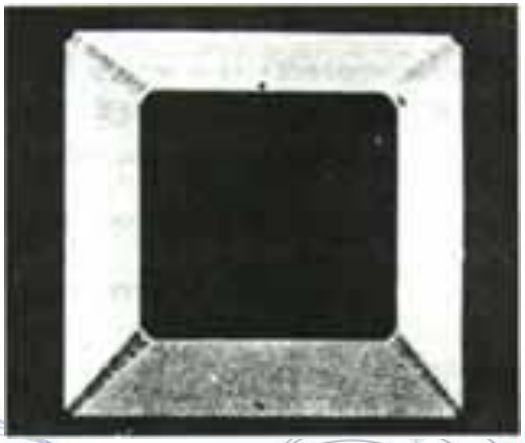


Wet Etch (5) — Corner Compensation



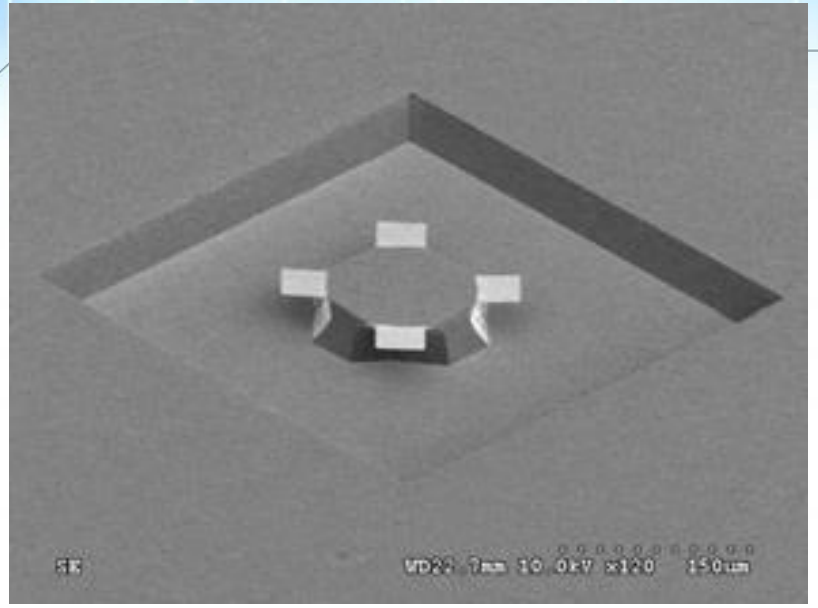


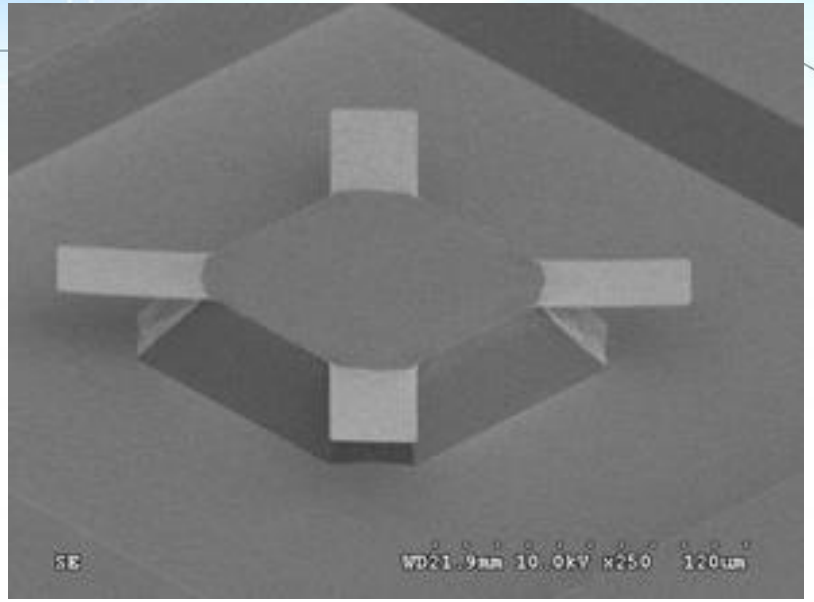


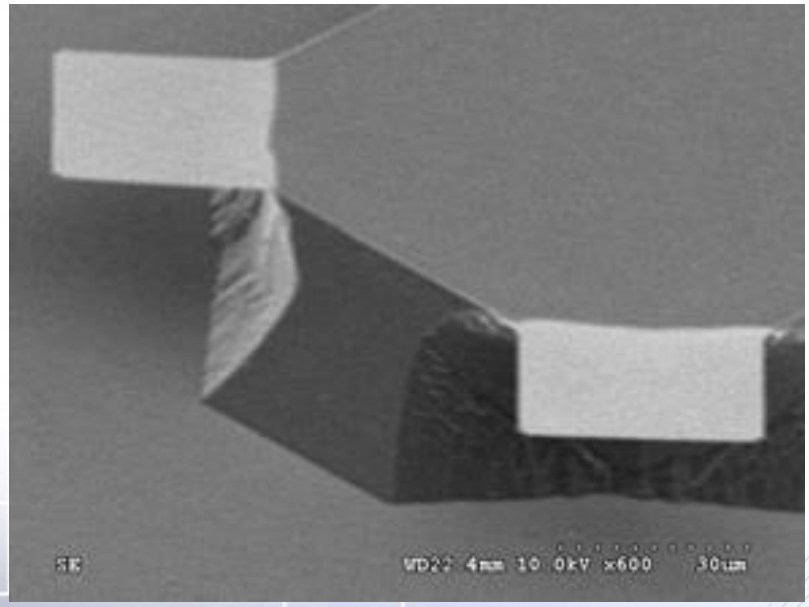


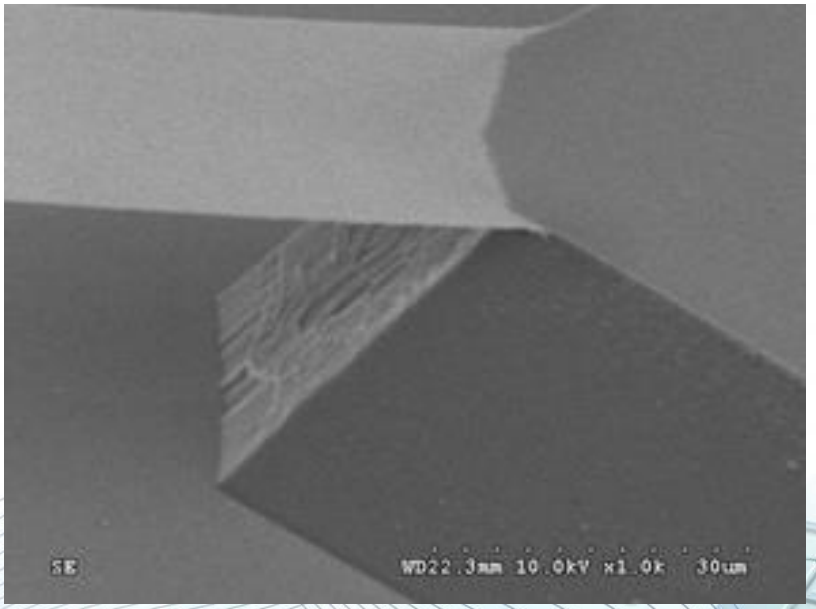
EDP etchant

KOH etchant

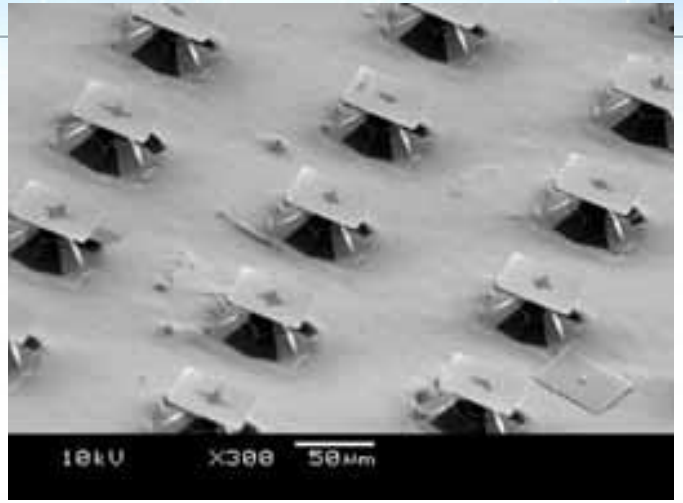

SE
WD22.7mm 10.0kV x120 150um

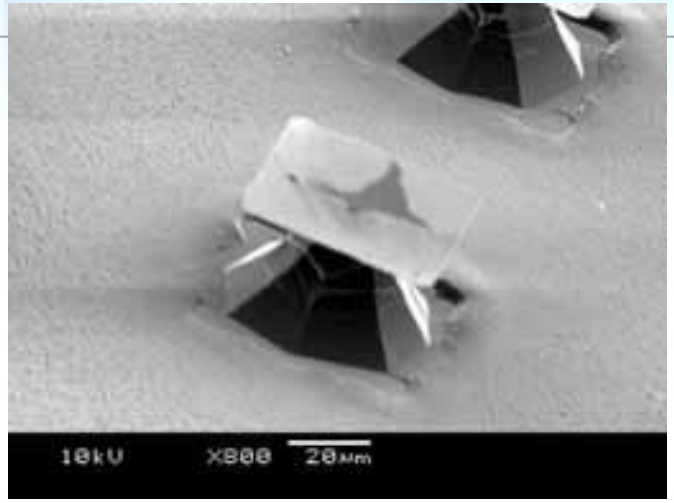

SE
WD21.9mm 10.0kV x250 120um


SE
WD22.4mm 10.0kV x600 30um

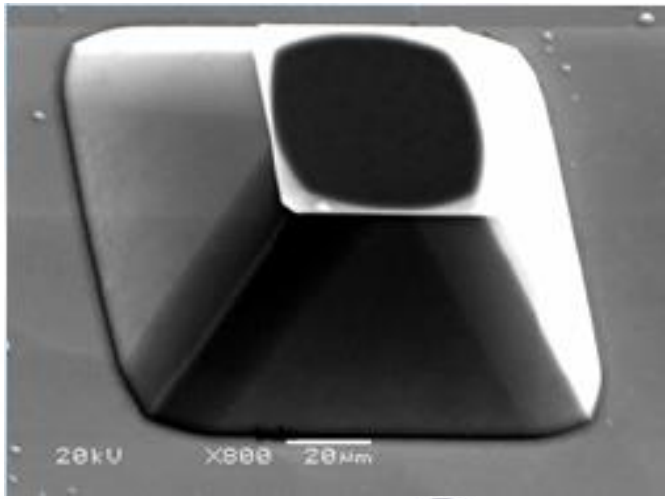

SE
WD22.3mm 10.0kV x1.0k 30um

Pure TMAH



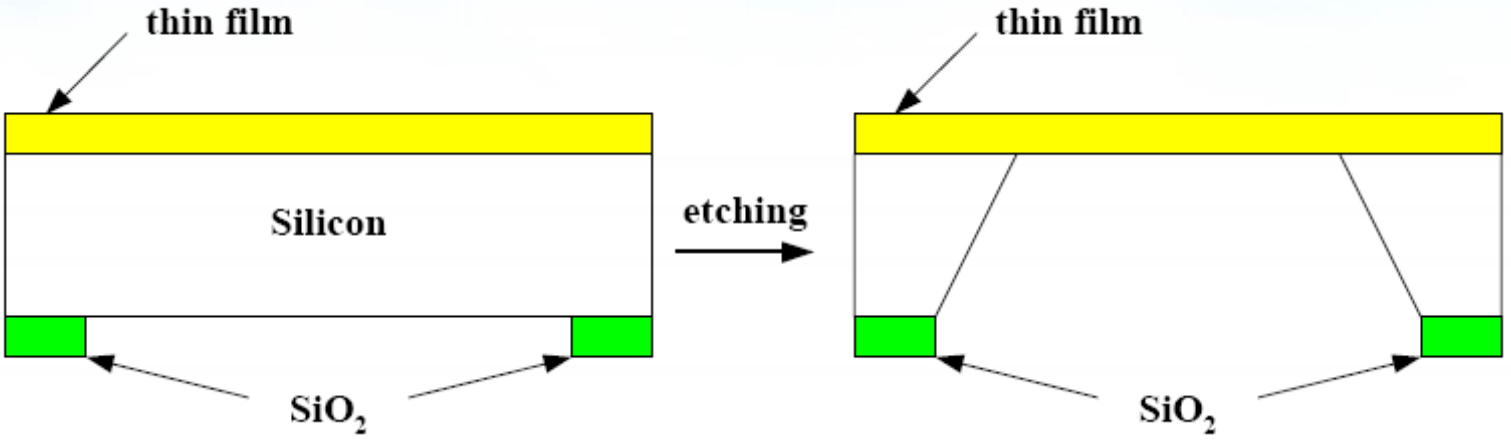


BR-Added
(添加劑)



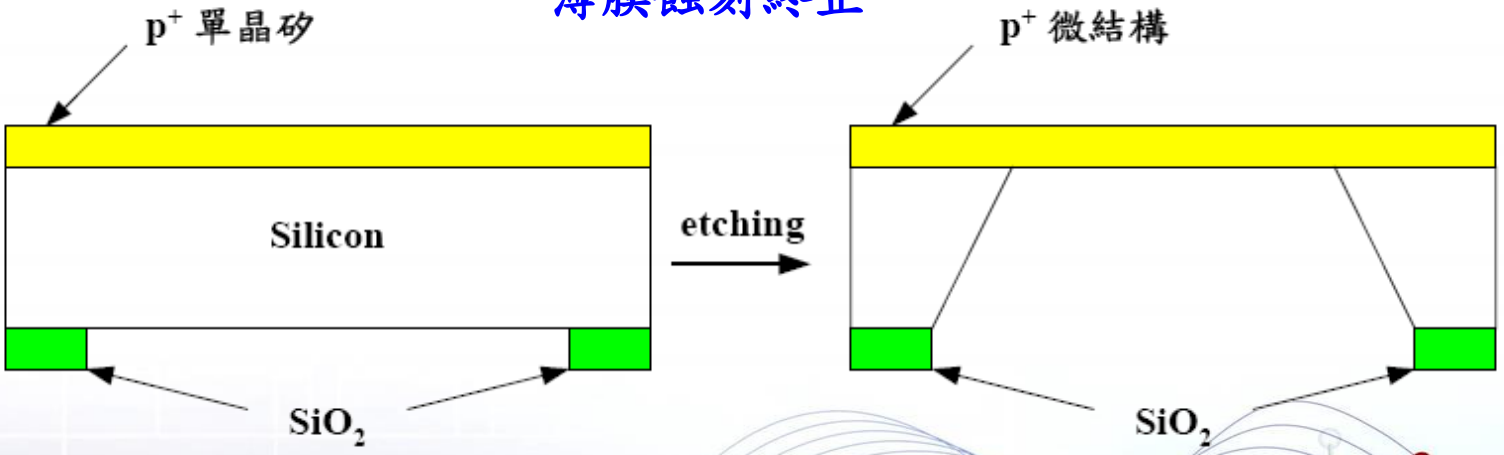
Mesa microstructures etched in TMAH-BR solution and pure solution without using the corner compensation technique.

Wet Etch (6) — Etching stop technology



必須使用雙面拋光晶片

薄膜蝕刻終止



摻雜蝕刻濃度終止

蝕刻率與摻雜物質的型態及摻雜濃度有關

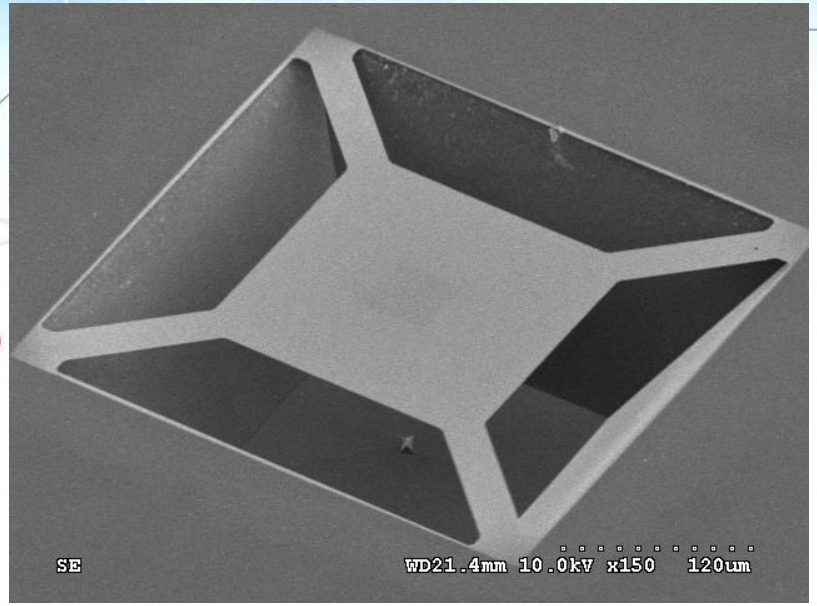
(a)金字塔結構

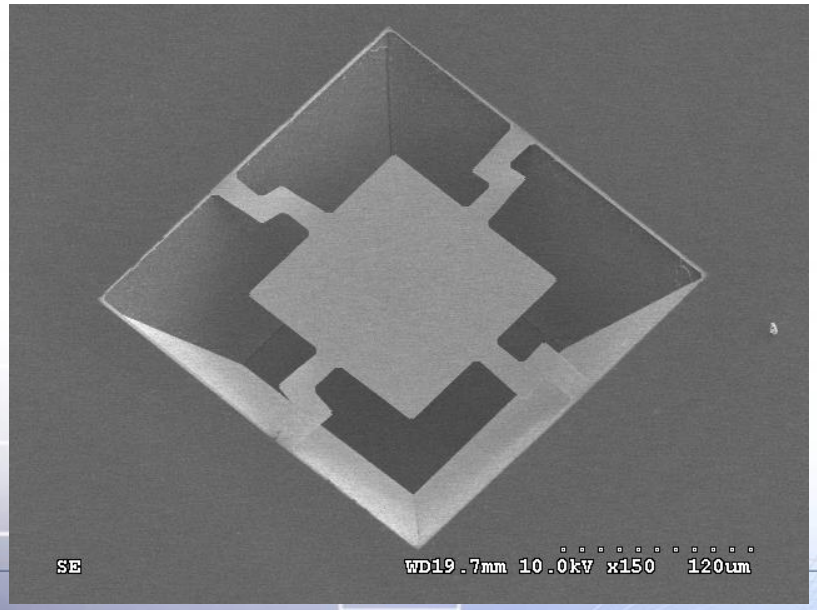
(b) 皺狀結構

(c) 微探針結構

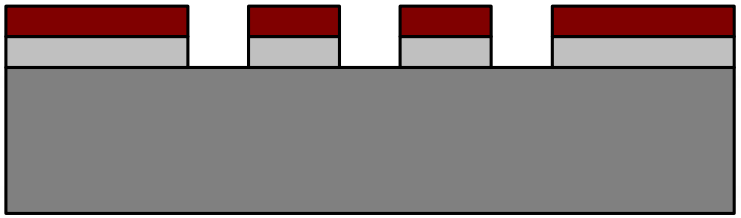
(d) 碗狀結構

利用非等向溼式蝕刻技術所蝕刻之各種薄膜微結構

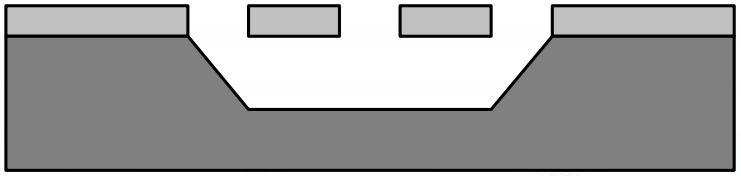




(a) LPCVD沉積Si_3N_4



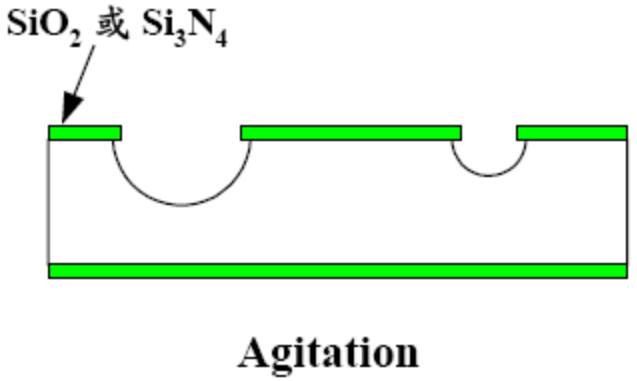
(b) 微影及用RIE蝕刻Si_3N_4



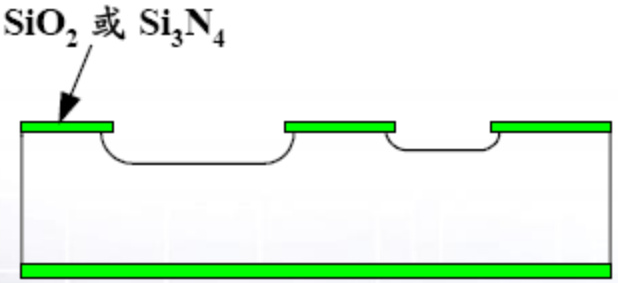
(c) 在KOH蝕刻液中蝕刻

Wet Etch (7) — 3-D 結構的限制

- 受限於單晶矽的鑽石立方結晶，蝕刻出來的角度是特定而無法改變的，不能蝕刻出特殊形狀的微結構，所以設計元件時就得考慮結構上的基本限制。



Agitation



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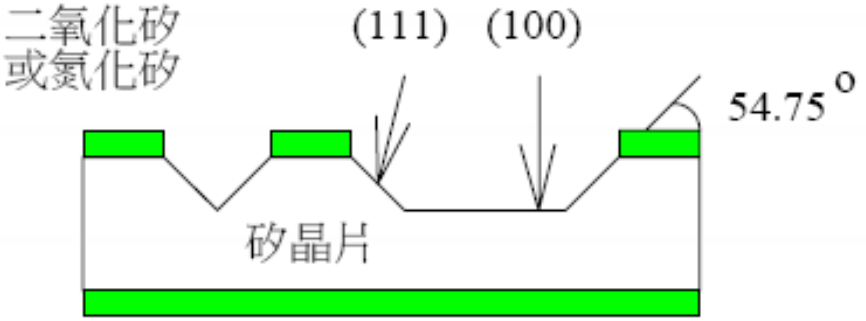
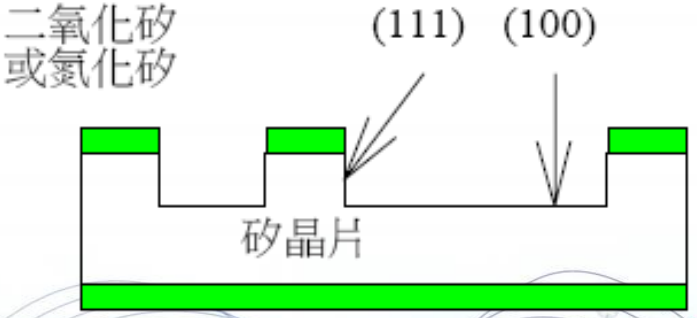
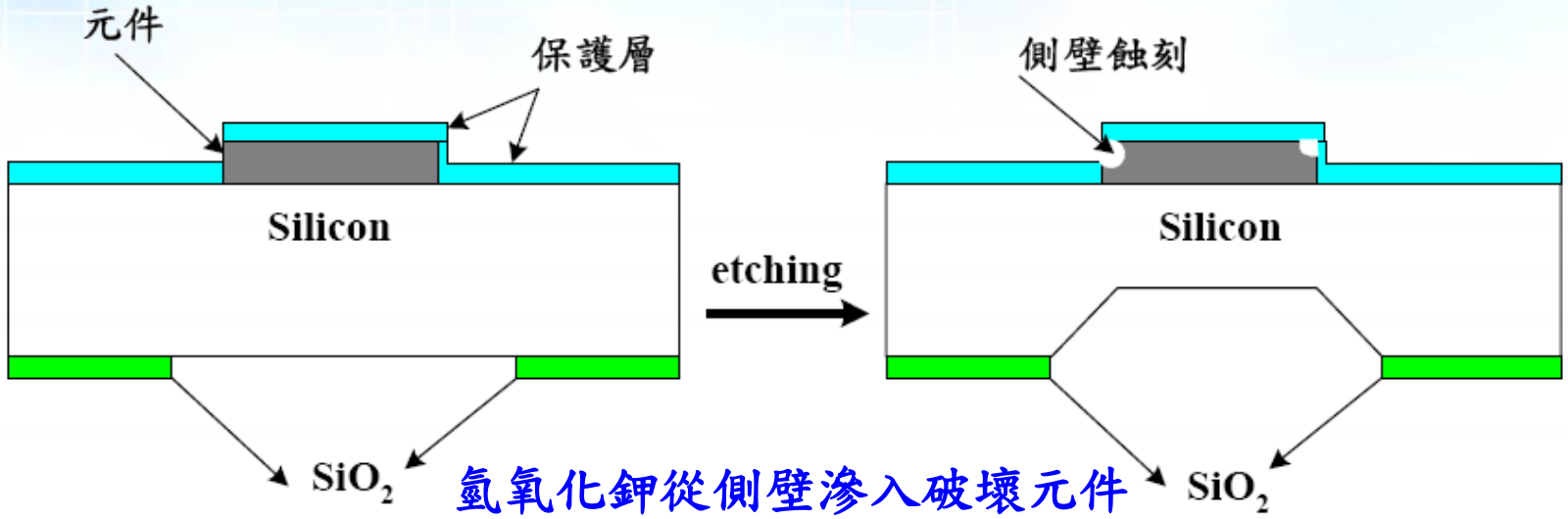


(a) <100>矽晶片

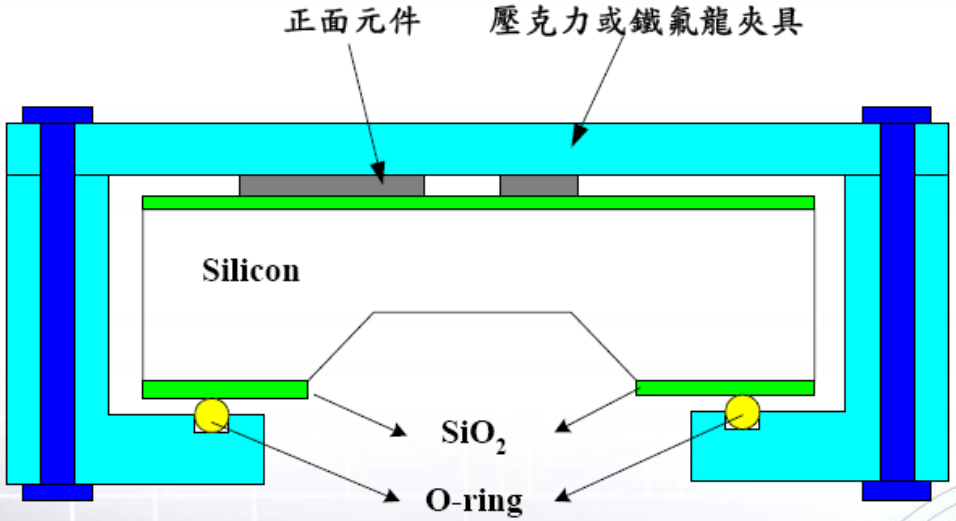


(b) <110>矽晶片

Wet Etch (8) — 蝕刻保護的必要性



氫氧化鉀從側壁滲入破壞元件



利用鐵氟龍或壓克力夾具保護正面的元件

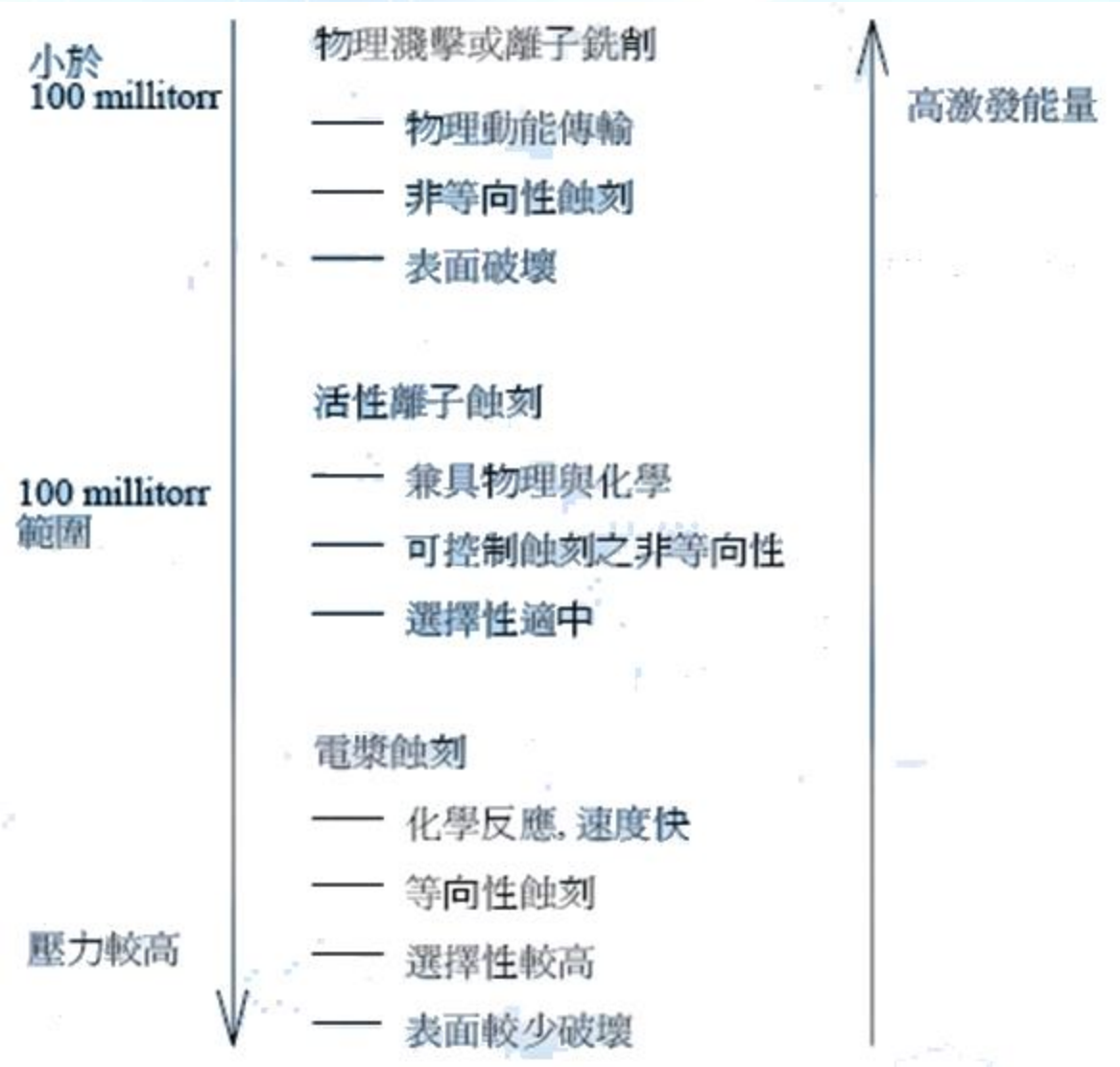
鐵氟龍夾具

矽乾式蝕刻技術

Silicon Dry Etching Technique

Dry Etch (1)

- 乾蝕刻沒有液態的蝕刻溶液，主要分為物理濺擊或離子銑削、電漿蝕刻、與介於兩者之間的活性離子蝕刻三類，右圖是三者蝕刻特性與壓力、激發能量的分類關係圖。



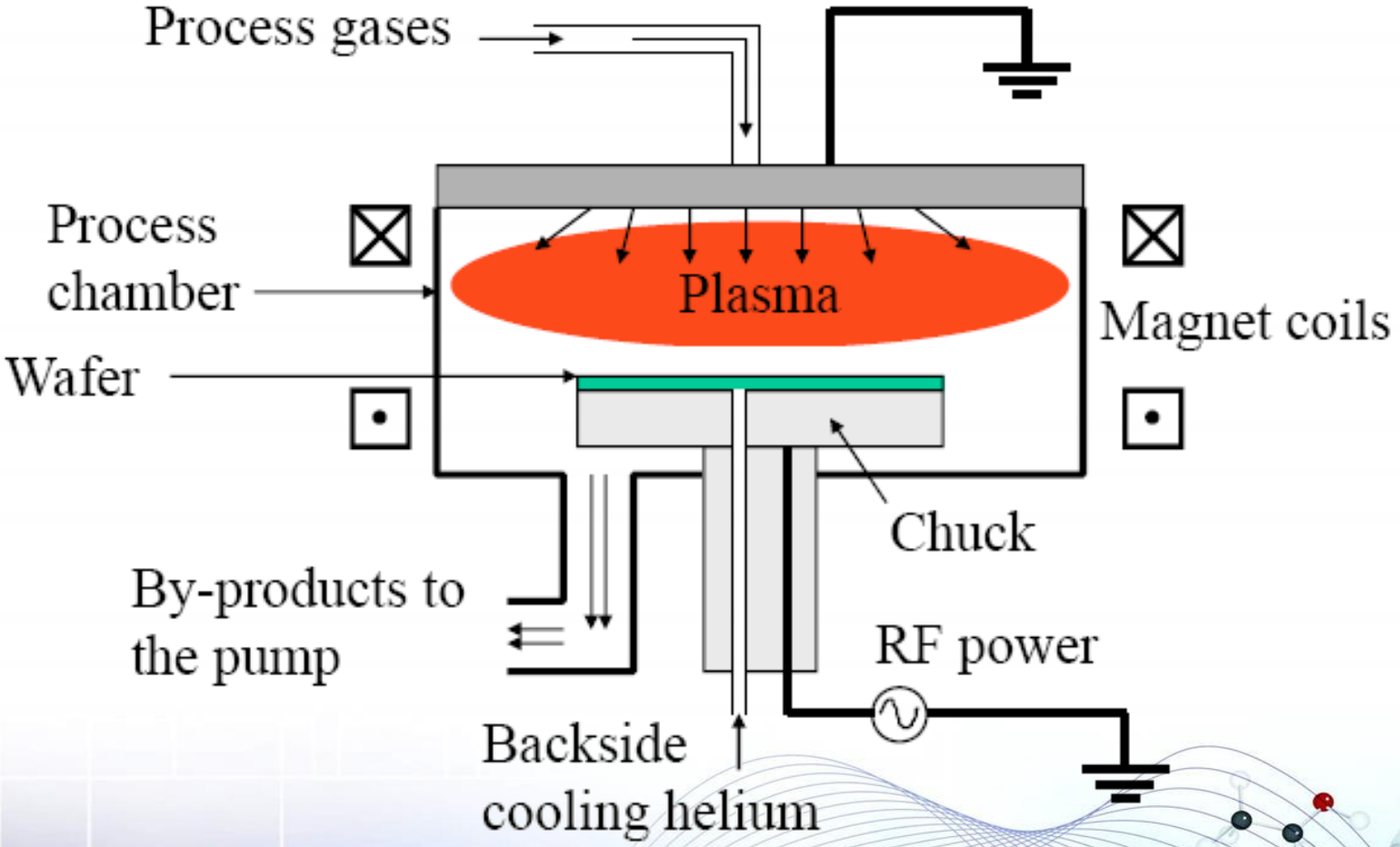
物理濺擊或離子銑削、電漿蝕刻、與活性離子蝕刻之關係

Dry Etch (2) — RIE and ICP

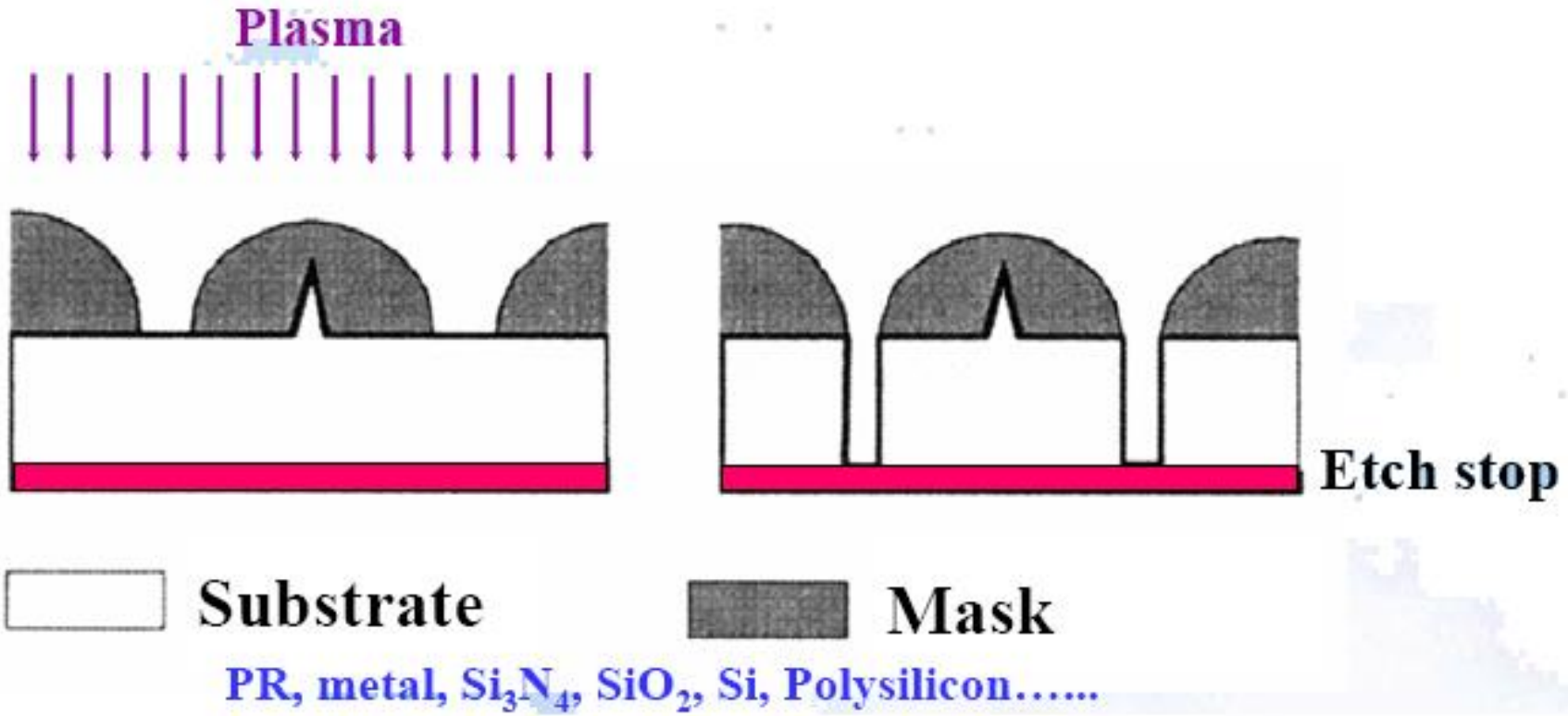
反應性離子蝕刻(RIE)系統,
NTNU MOEMS Lab.

感應耦合電漿蝕刻(ICP-RIE)系統,
PIDC

Dry Etch (3) — 活性離子蝕刻系統示意圖

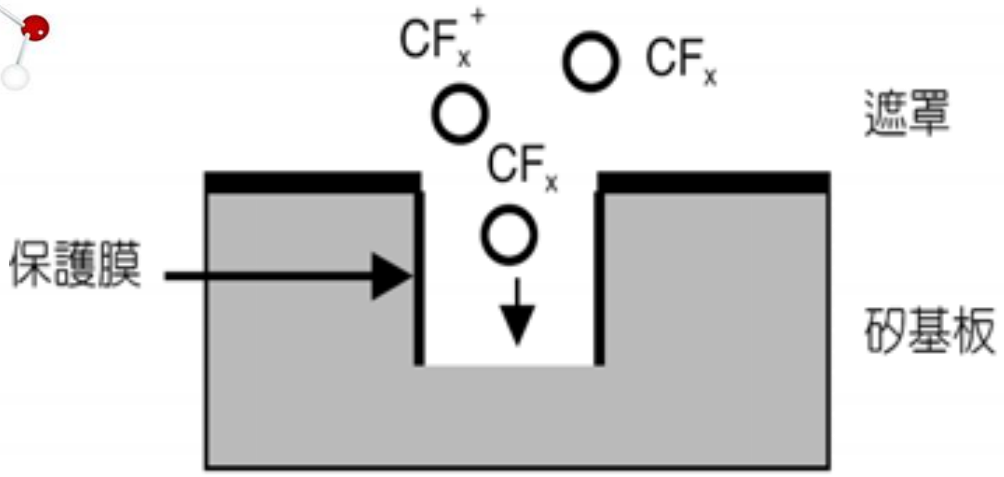


Dry Etch (4) — 電漿蝕刻

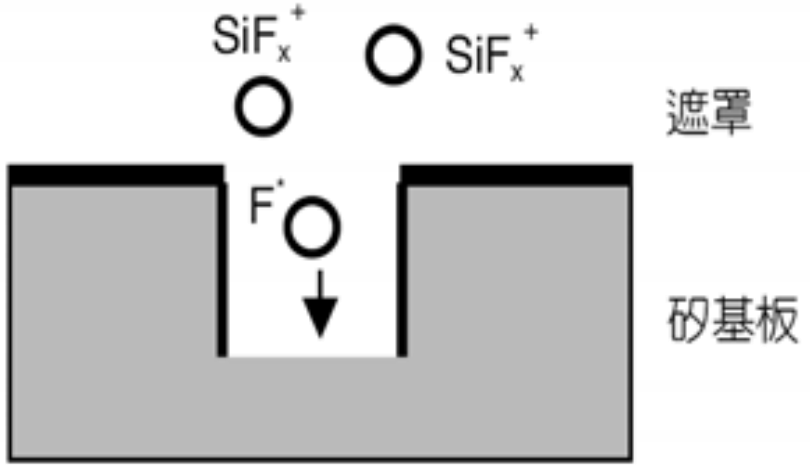


Mask材料選擇的原則：高選擇比, 蝕刻深度, 非等向性…

Dry Etch (5) — 蝕刻原理

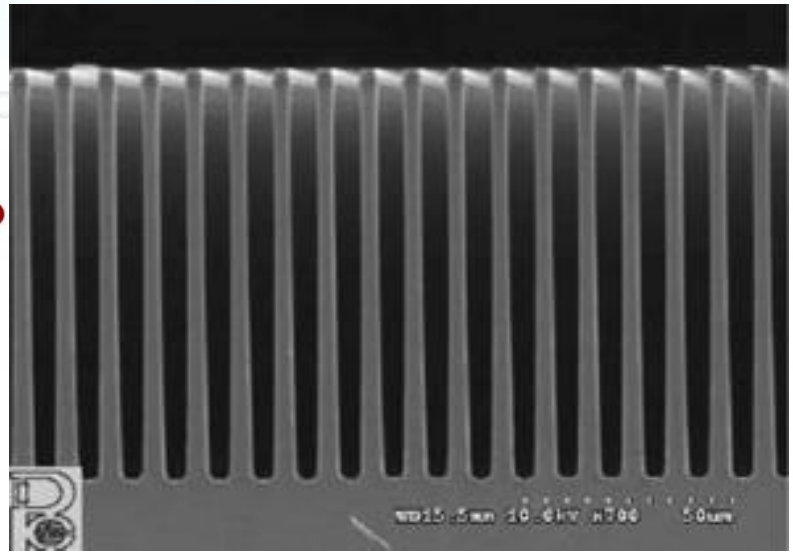


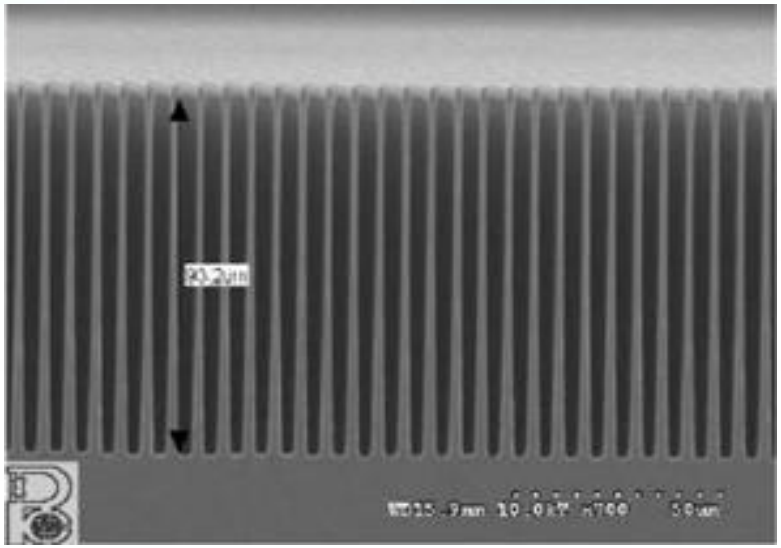
保護製程步驟

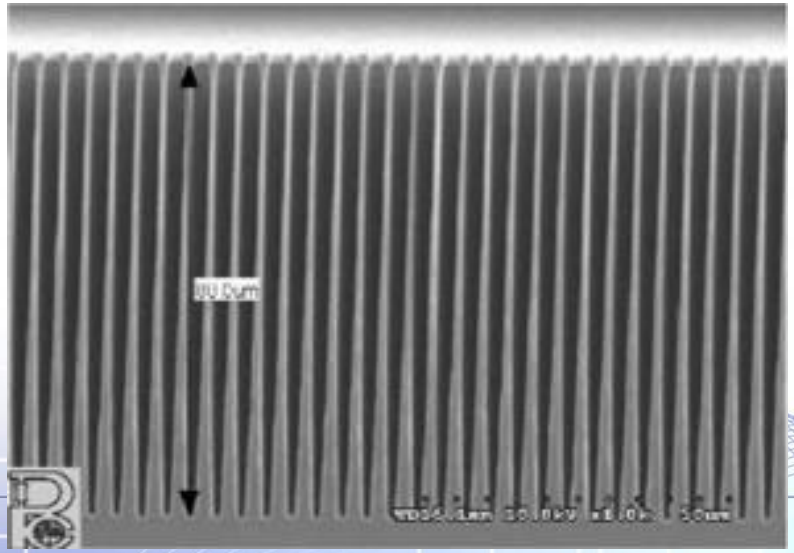


蝕刻製程步驟

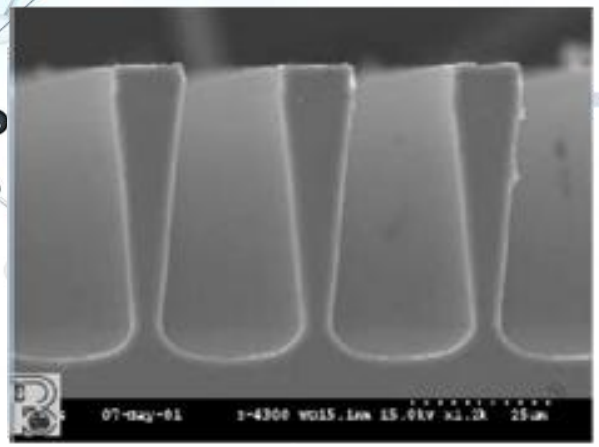
Dry Etch (6) — ICP-RIE SEM圖



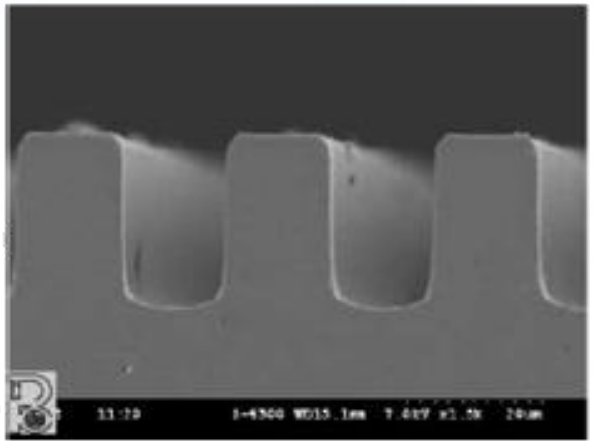




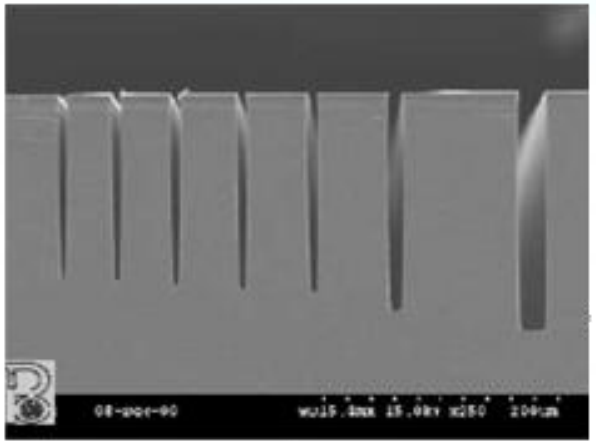
Dry Etch (6) — ICP-RIE 缺陷



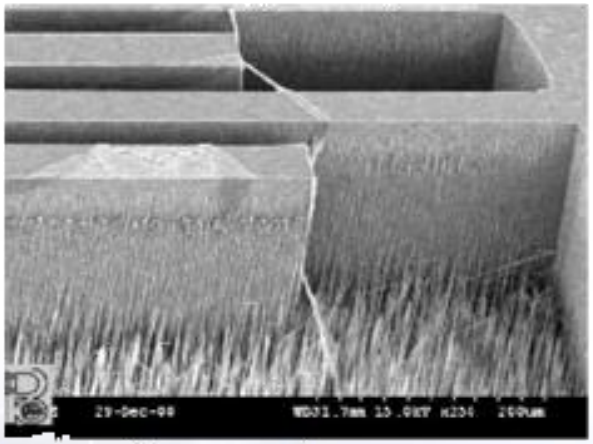
蝕刻溝槽外擴



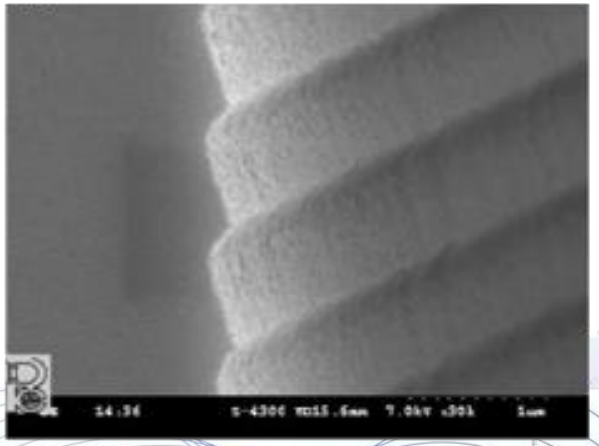
蝕刻溝槽內凹



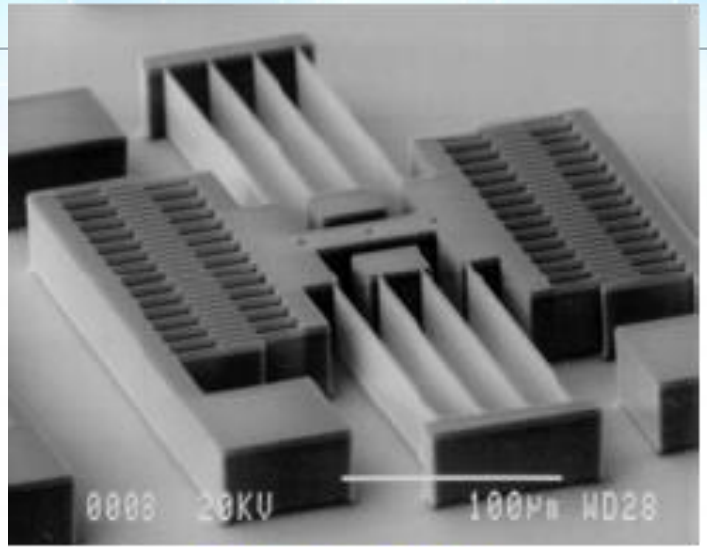
蝕刻延遲



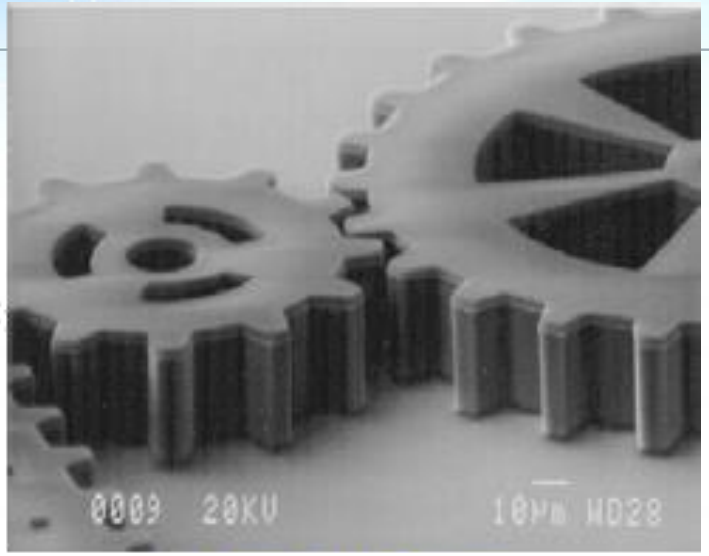
雜草現象



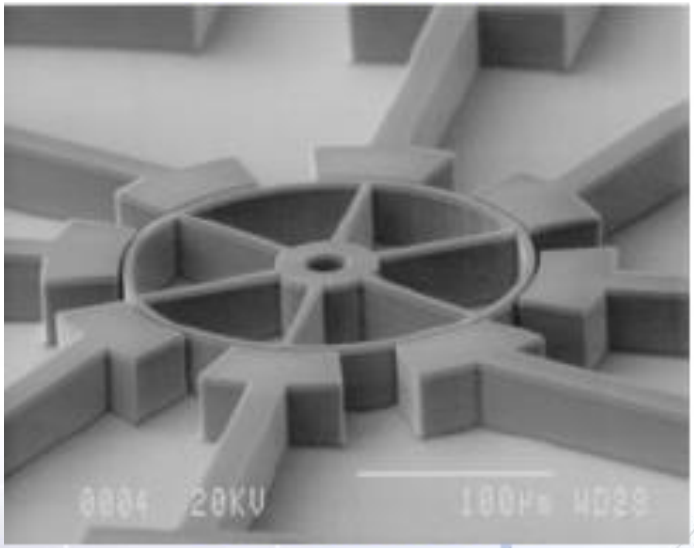
側壁橫紋



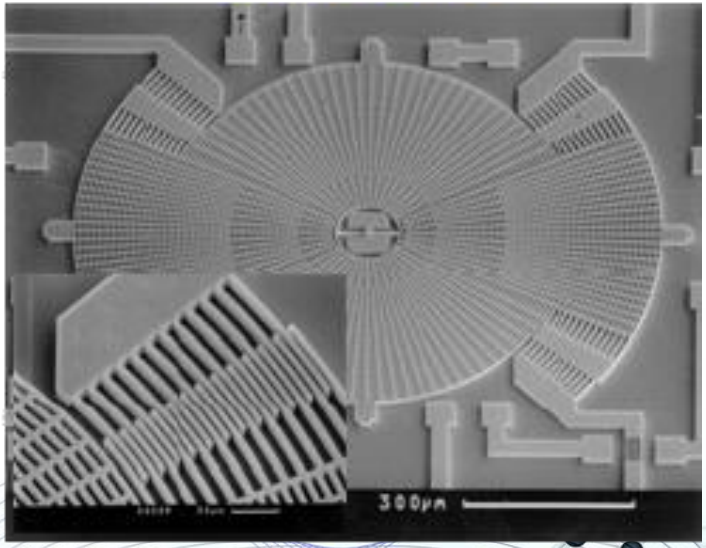
Comb-driver



Nested Gears



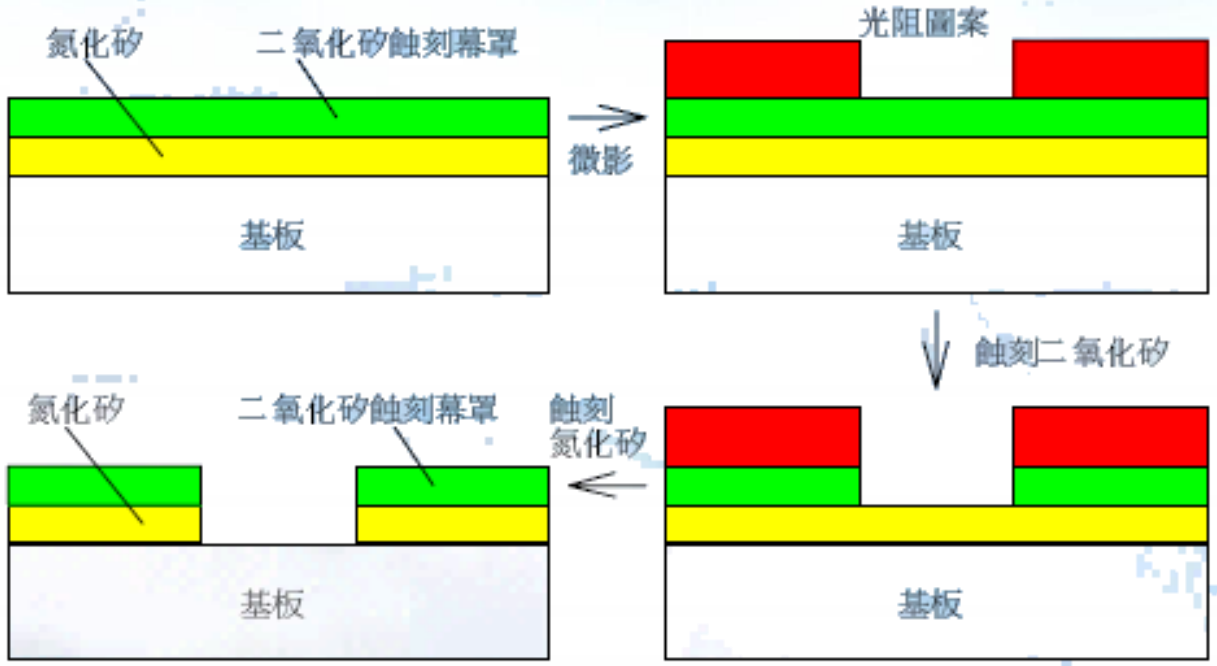
Micromotor



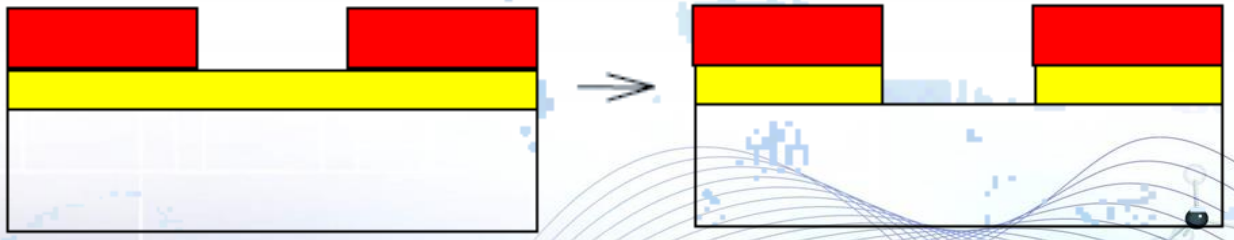
Gyroscope

MCNC, USA

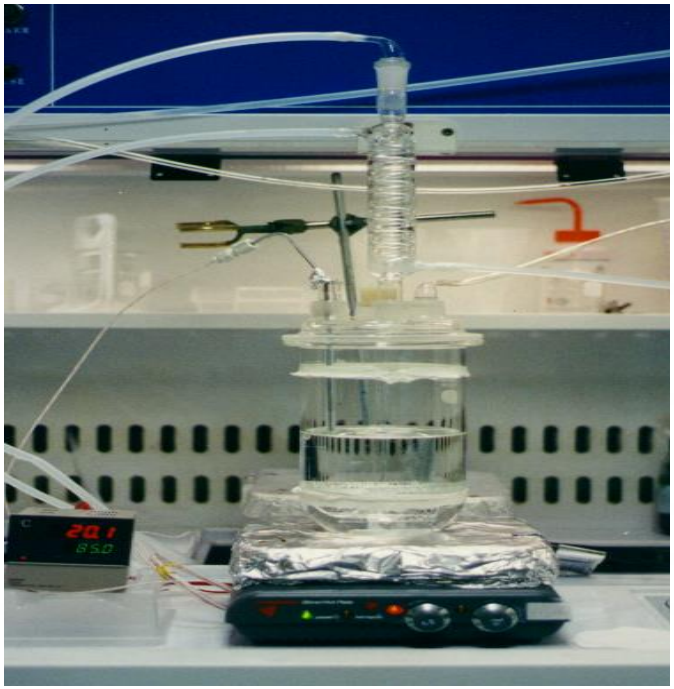
氮化矽乾、溼式蝕刻的差異性



溼式蝕刻：H_3PO_4(85%)@175℃



乾式蝕刻：CF_4(10 sccm)@60 mTorr



濕式蝕刻裝置(成本低)

感應耦合電漿蝕刻(ICP-RIE)系統,
ITRC（成本極高）

LIGA,UV-LIGA,SIGA

LIGA與LIGA-Like製程與應用技術

MEMS領域中微製造技術分類表

<table>
<tr><td rowspan="6">非矽基微加工</td><td>LIGA技術</td><td colspan="2">X-ray深光刻術</td><td>精密電鑄技術
•純金屬電鑄
•合金電鑄</td><td>微微成形技術
• 塑膠微結構成形
熱壓成形、射出成形
輪壓成形、紫外線硬化法
•陶瓷微結構成形
粉末射出成形、 帶板鑄造</td></tr>
<tr><td>LIGA-like
技術</td><td colspan="2">紫外光厚膜光阻微影
準分子雷射微加工
感應耦合電漿離子蝕刻*
電子束光刻術</td><td colspan="2"></td></tr>
<tr><td rowspan="3">微機械加工</td><td>切削加工</td><td colspan="3">微切削加工、微鑽孔加工、微銑削加工、微輪磨加工</td></tr>
<tr><td>非切削加工</td><td colspan="3">微電鍍成形、微壓模成形、微射出成形、微沖壓成形</td></tr>
<tr><td>特殊加工</td><td colspan="3">微放電加工、雷射微加工、離子束微加工、電子束微加工、
超音波微加工、原子力顯微加工術</td></tr>
<tr><td>高分子微加工
技術</td><td colspan="4">微雷射光合高分子成形(Microstereolithography, μ-SL)
軟式微影技術(Soft Lithography)
微接觸印刷術(Microcontact Printing, μ-CP)
Micromolding in Capillaries (MIMIC)
Microtransfer Molding (μ-TM)
Replica Molding (REM)</td></tr>
<tr><td>其他低溫製程技術與材料</td><td colspan="4">聚對二甲苯(Parylene)、明膠(Gelatin)蛋白質、鐵氟龍(Teflon)、矽膠(Silicone)</td></tr>
</table>

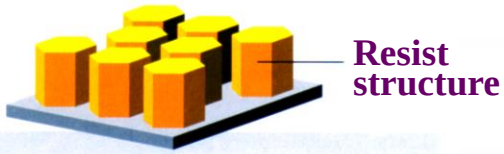
註：感應耦合電漿離子蝕刻技術通常歸類為非等向性高深寬比矽基蝕刻技術。

LIGA製程：

Lithographie:光刻
Galvanoformung:電鑄
Abformung:模造

1. 光刻

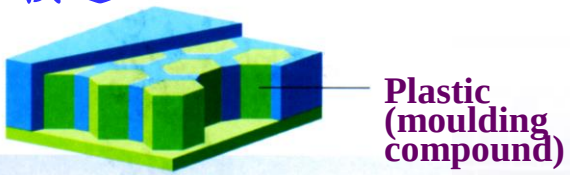
2. 顯影



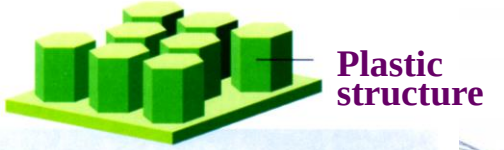
3. 電鑄

4. 金屬模仁

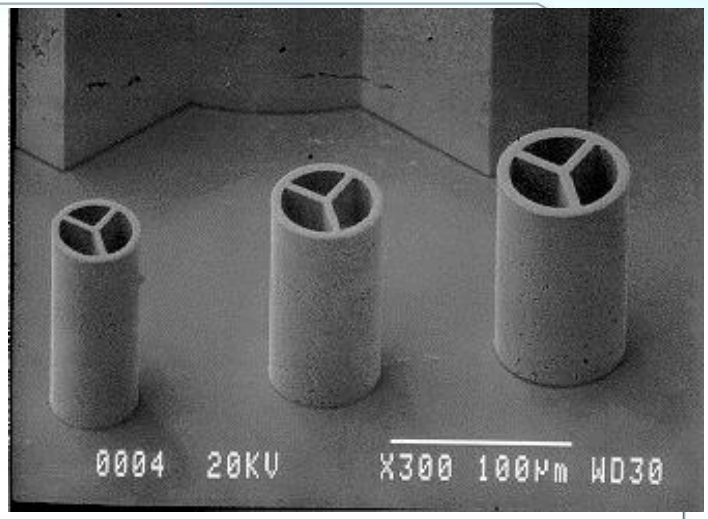
5.模造



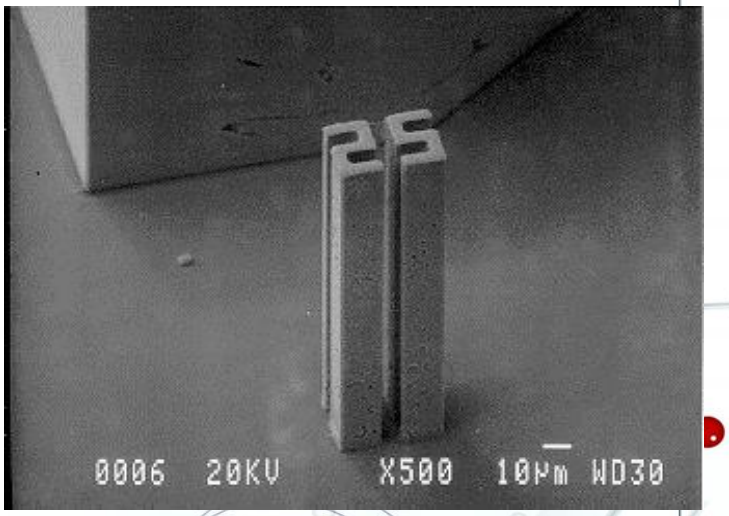
6. 脫模



Source: Institut für Mikrotechnik Mainz (IMM), Germany

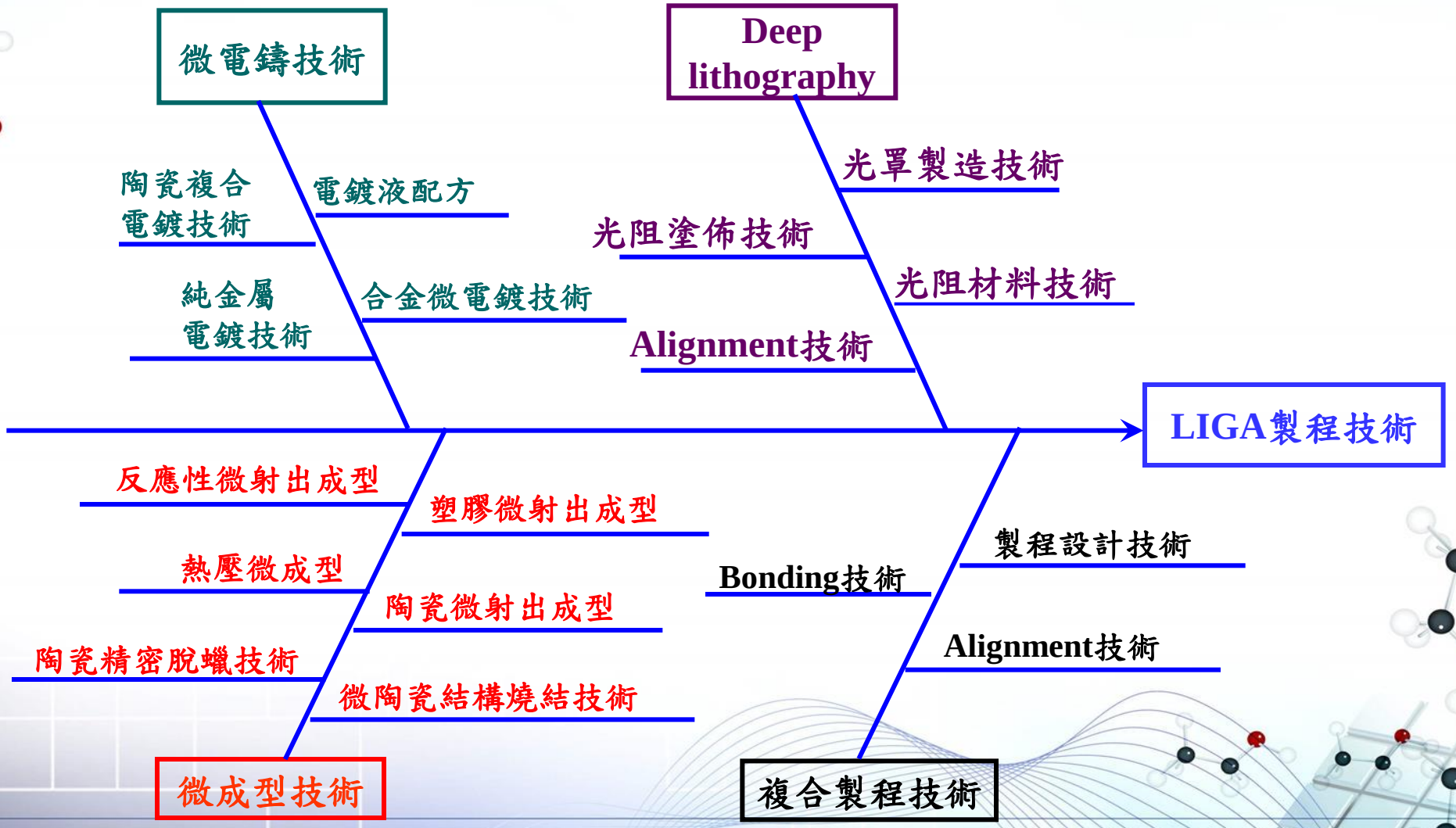


MCNC



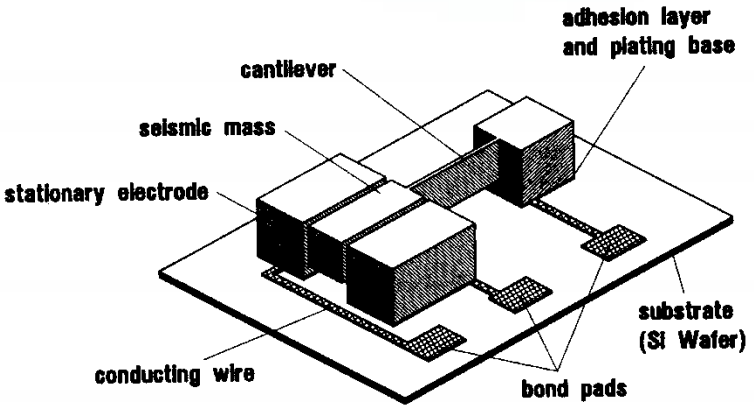
高深寬比(high aspect ratio)的微結構

LIGA製程技術的技術關聯圖

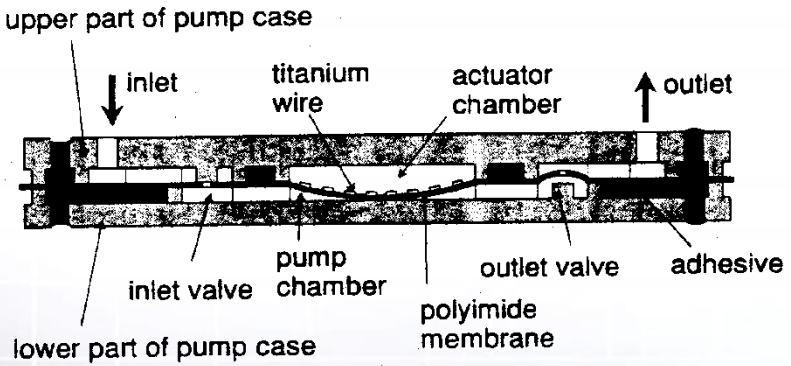


犧牲層LIGA (S-LIGA)技術的應用範圍

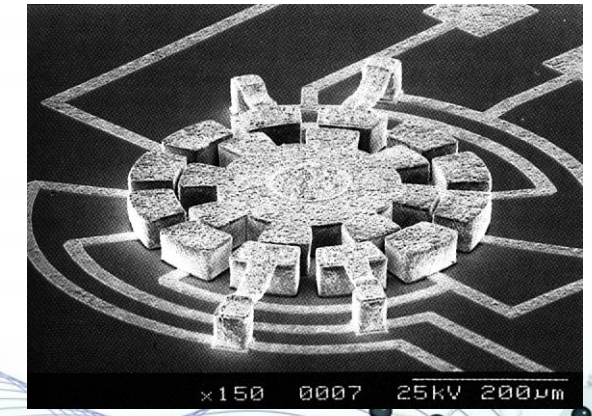
- 微感測器的懸浮結構
- 可控制流量進出的微閥門
- 各型微致動器的移動或轉動結構等.....



Acceleration microsensor



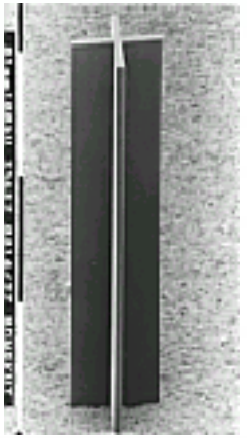
Micropump

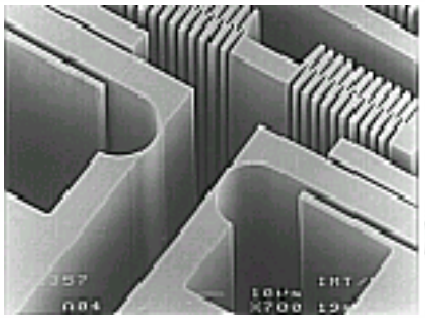


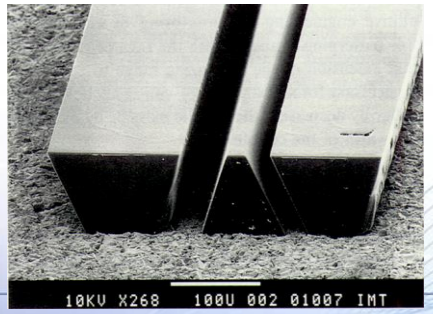
Micromotor

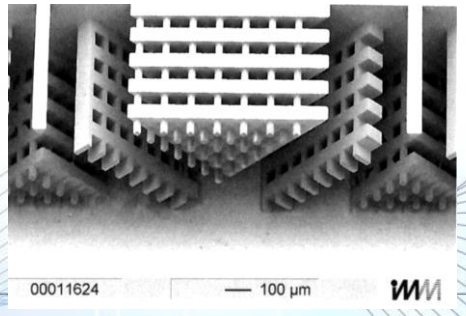
Key Features of X-ray LIGA Microstructures

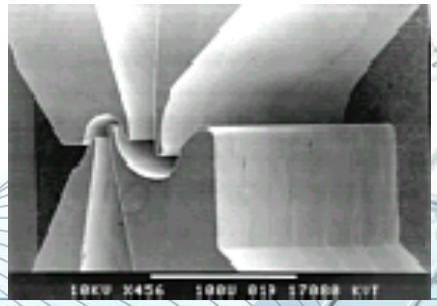
- **Realization of arbitrary shape**
- **Extreme structure height (>mm)**
- **Extreme aspect ratio (>100)**
- **Minimum lateral dimensions 0.5±0.1μm**
- **Surface roughness 0.03-0.05 μm**
- **Vertical & smooth sidewalls**
- **Wide variety of materials**
- **Successful in mass fabrication**











IMT and IMM, Germany

LIGA 製程 vs. 類LIGA 製程

光刻源的差異

LIGA 製程：同步輻射X光

- 加工深度數mm、次微米級精度、深寬比＞100
- 同步輻射光源為一龐大且昂貴的設備
- X-ray 光罩製作複雜且成本高

類LIGA 製程：低成本替代性光源

- 加工深度≦ 1mm、微米級精度、深寬比≦50
- 紫外光–厚膜光阻微影製程
- 準分子雷射
- 反應性離子蝕刻

Synchrotron Radiation Research Center (for LIGA process)

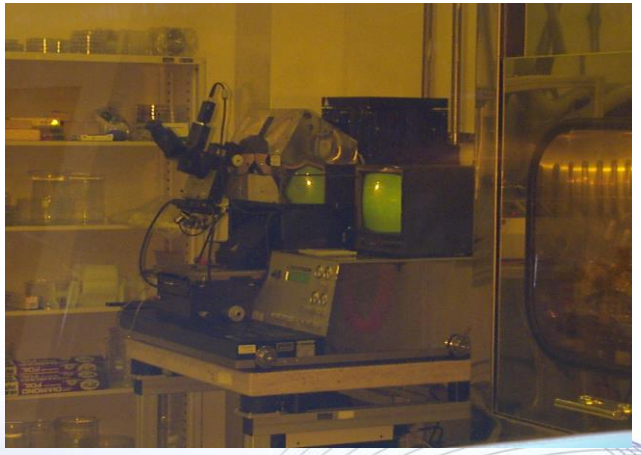
USA APS

FRANCE ESRF

JAPAN SPring-8

Low-cost Exposure System (for LIGA-like process)

Excimer Laser System

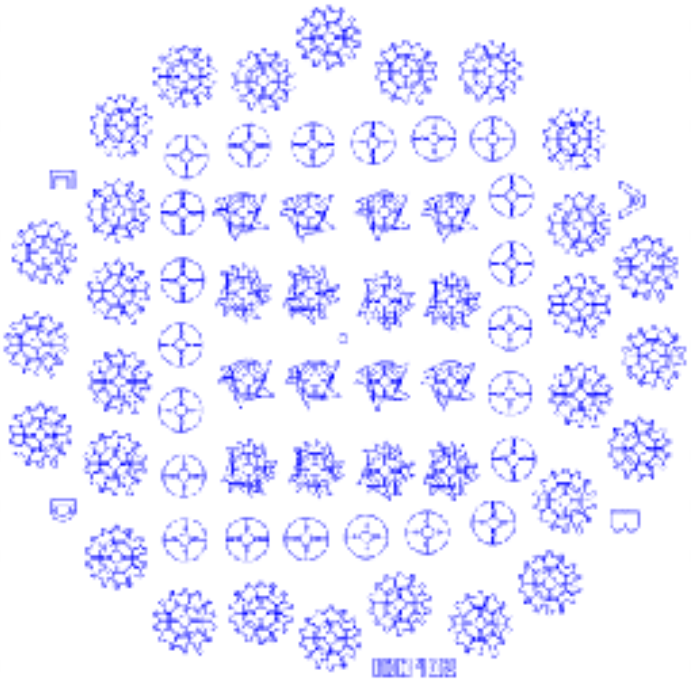


UV mask aligner

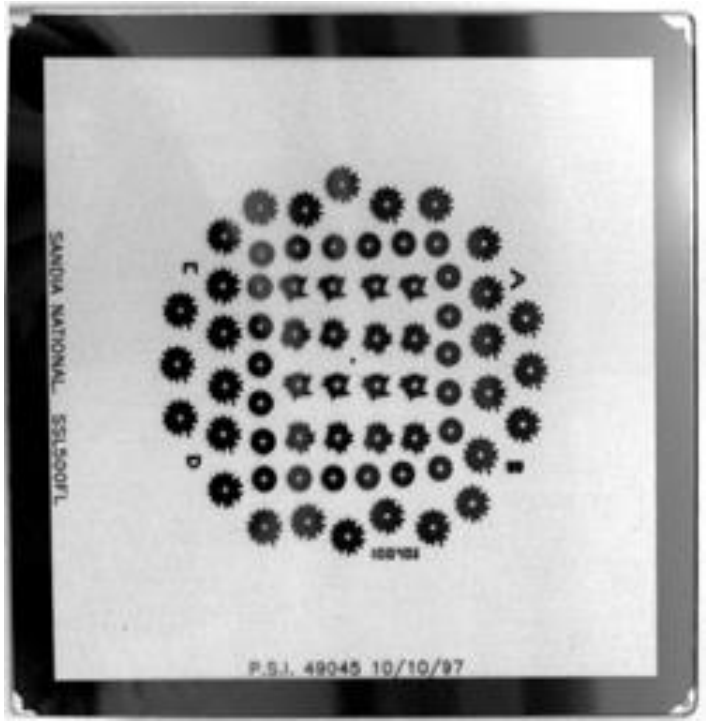
ICP-RIE System

Instrument Technology Research Center, ITRC

Photomask of UV Lithography



(a) CAD Layout



(b) Chrome Mask

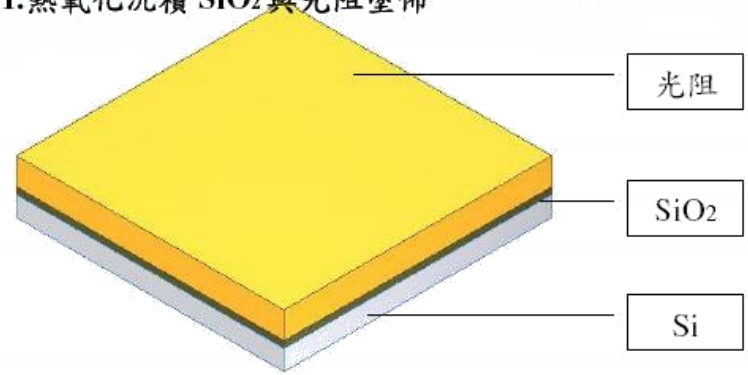
Source: http://daytona.ca.sandia.gov/LIGA/mask.html
(Sandia National Laboratory, USA)

SIGA製程

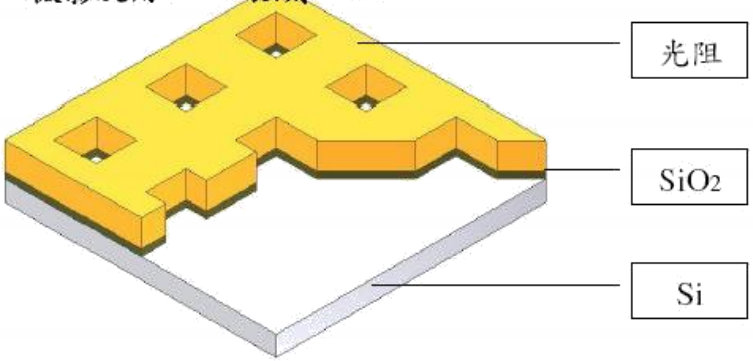
In German:
Silizum-mikrostrukyur
Galvanoformum
Abformung

In English:
Silicon-microstructuring
Electroforming
Molding

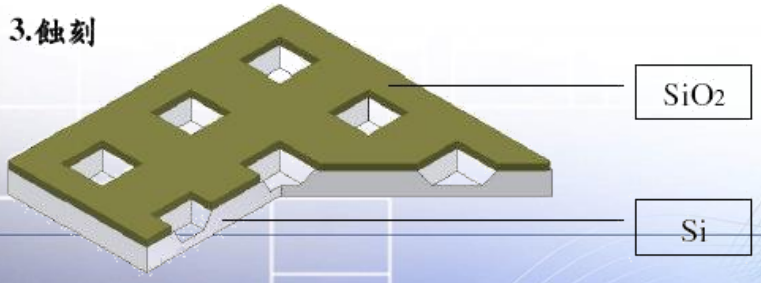
1.熱氧化沉積 SiO_2 與光阻塗佈



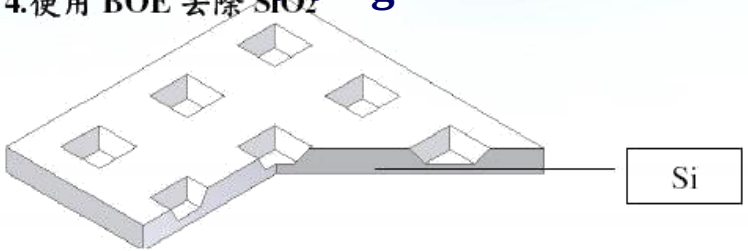
2.微影及用 BOE 蝕刻 SiO_2



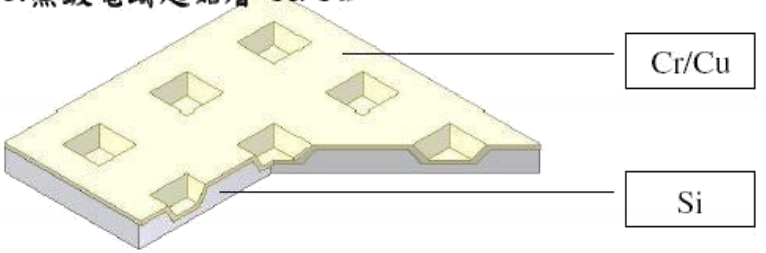
3.蝕刻



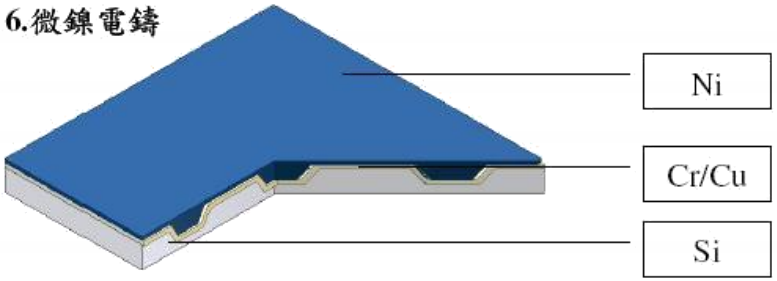
4.使用 BOE 去除 SiO_2



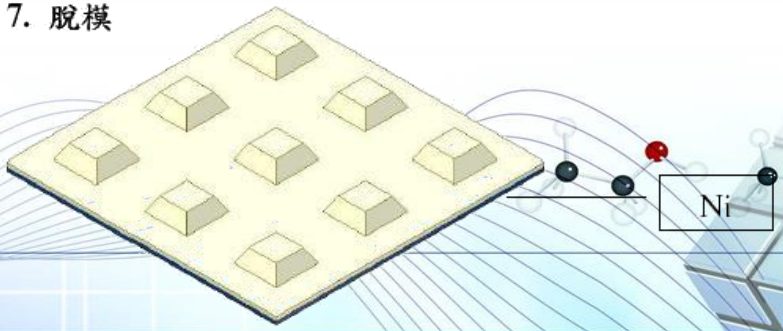
5.蒸鍍電鑄起始層 Cr/Cu



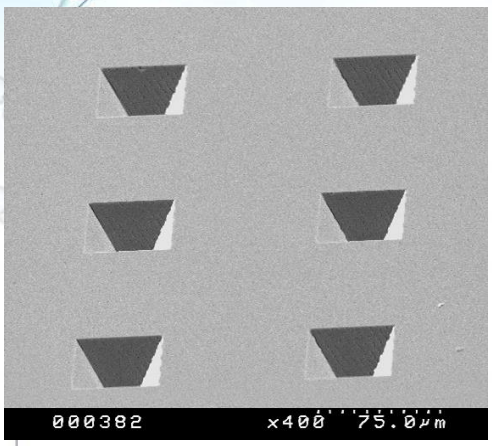
6.微鎳電鑄

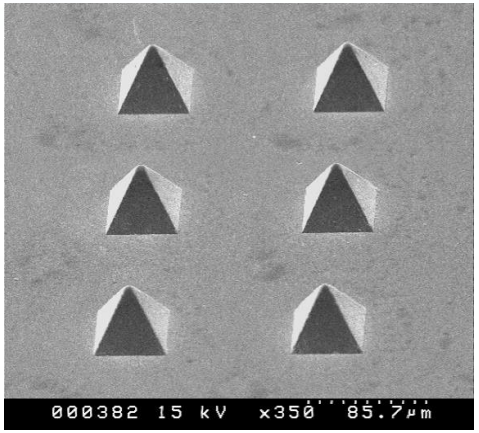


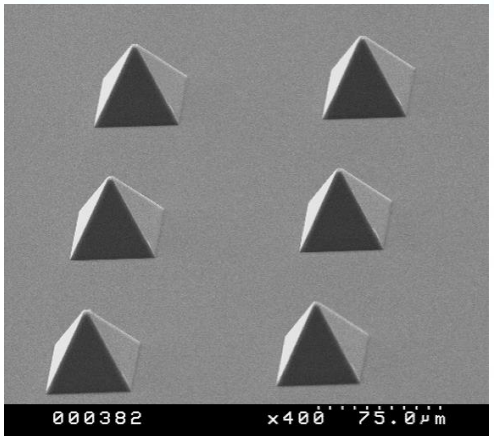
7. 脫模

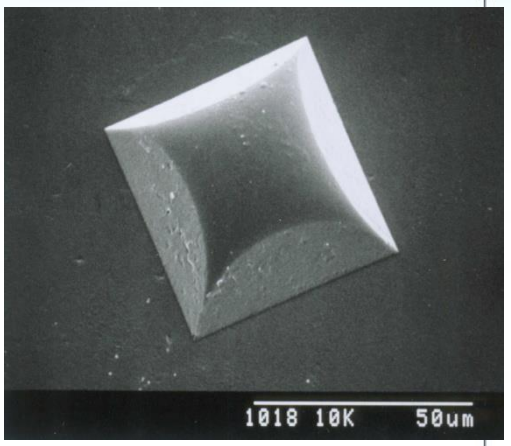


微結構充填不足

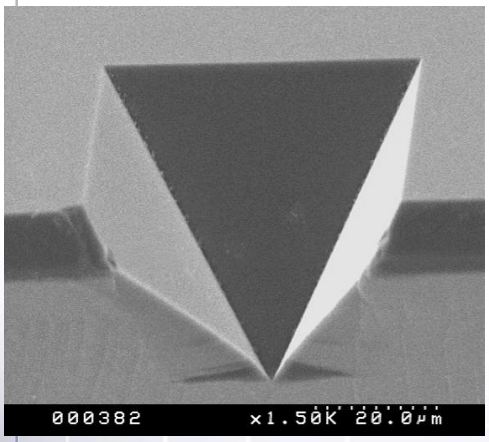




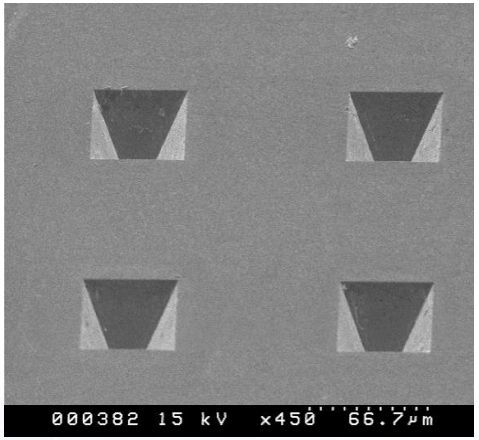




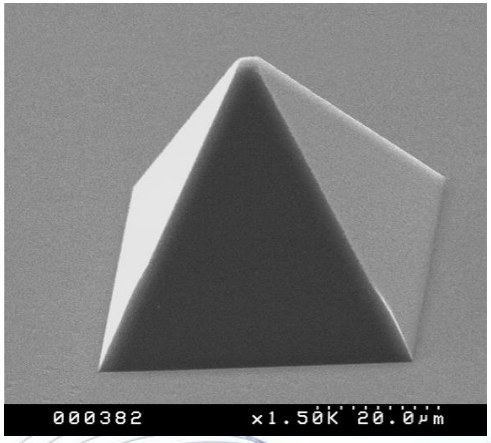
一次電鑄鎳模仁



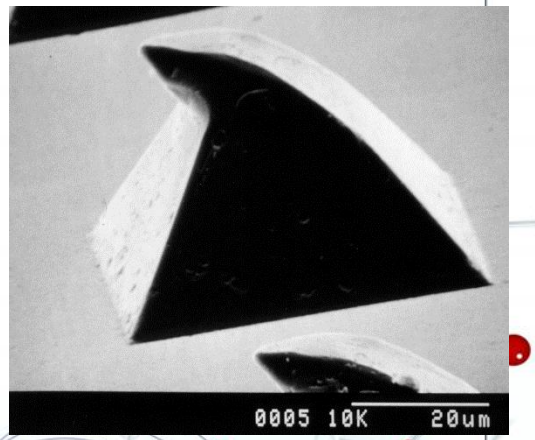
矽模仁



二次電鑄鎳模仁

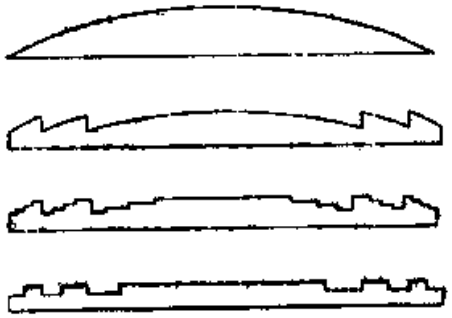


PMMA壓模成形

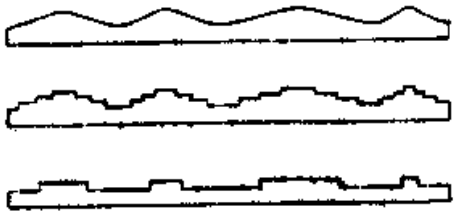


微結構收縮變形

SIGA製程應用技術(1)

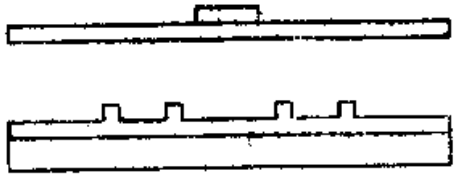


Lenses

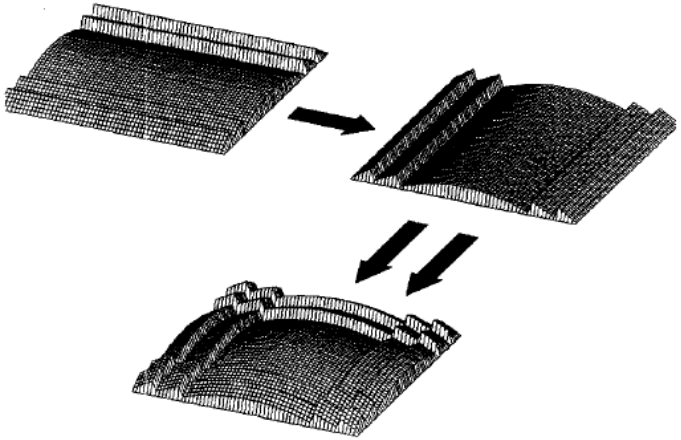


Holograms

Gratings

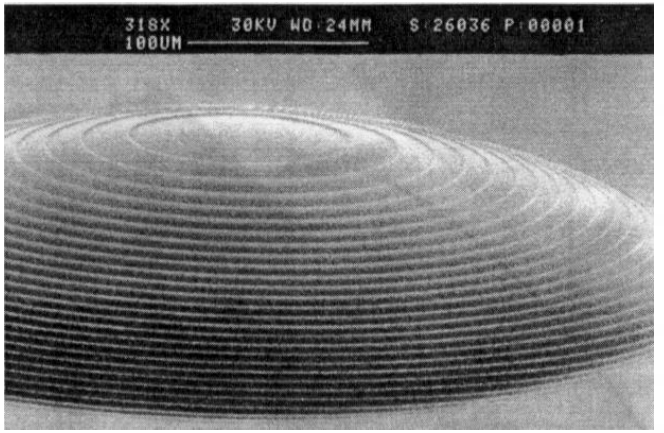


Waveguides

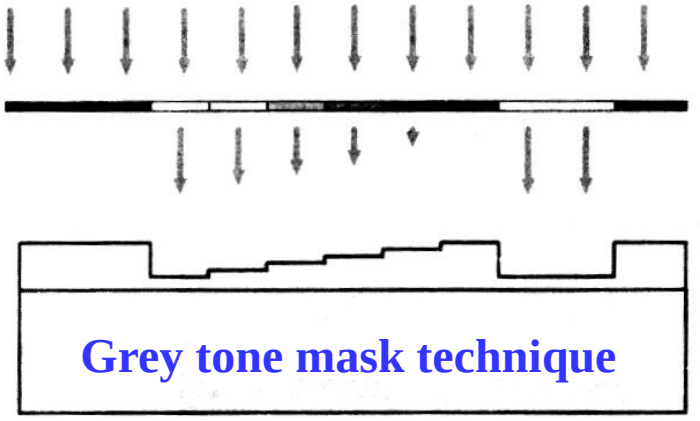


成形方法：

1. Lithography +RIE etching
2. Photoresist reflow
3. Direct writing of e-beam or laser
4. Shaped light beam method
5. Grey tone mask technique

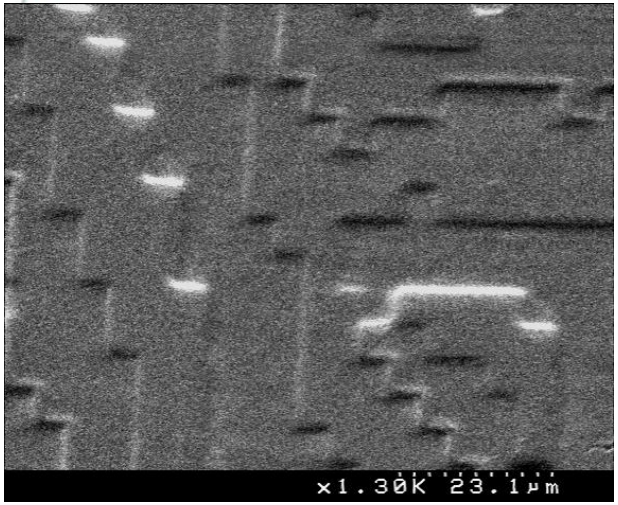


Direct writing of e-beam

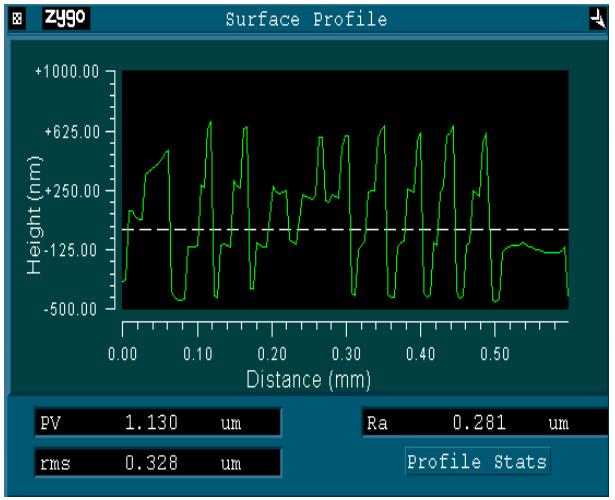


Grey tone mask technique

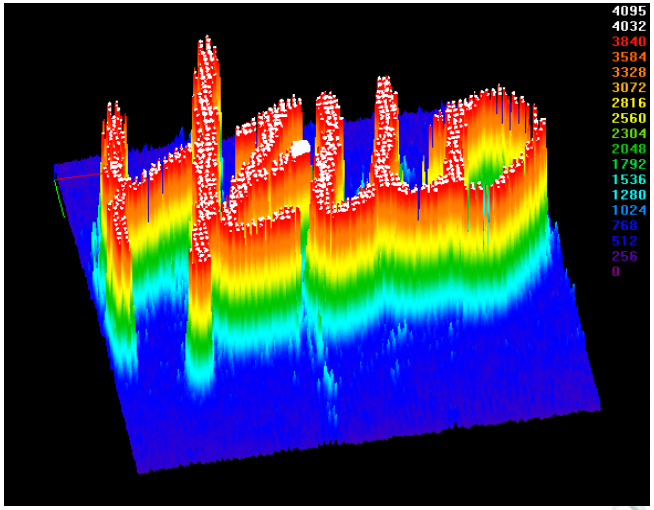
四階全像片應用



像素5 µm
四階全像片

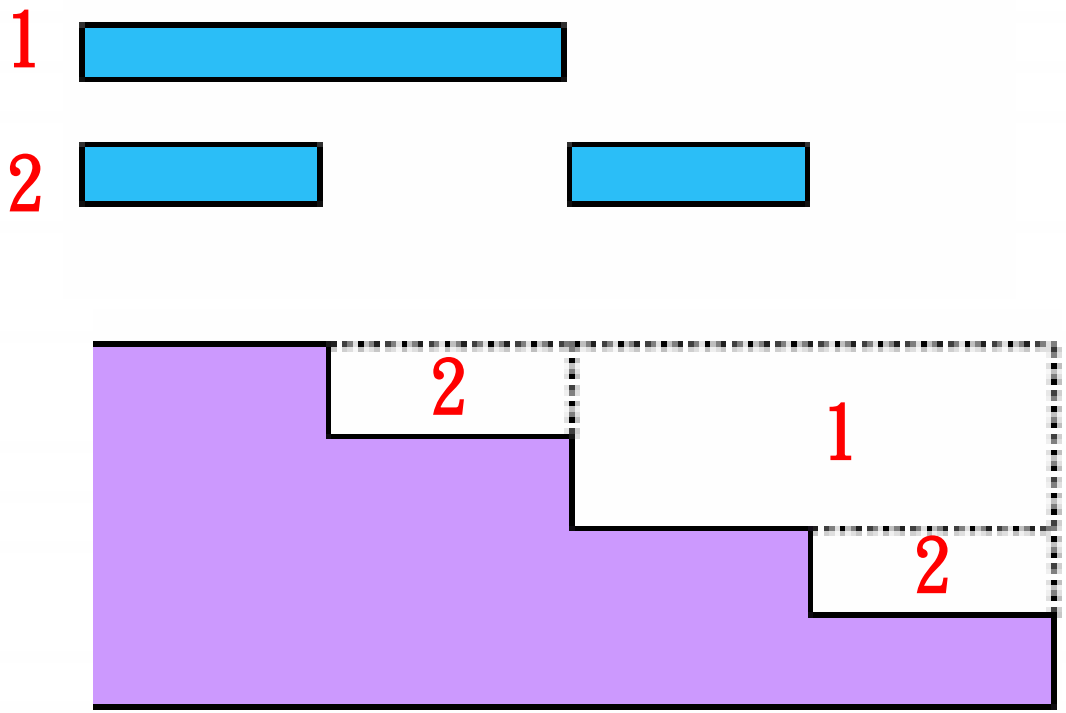


四階全像片α-
step圖



“HELLO”
影像輸出

四階全像片加工技術



四階光罩組合

全像片模仁製作流程圖

Si

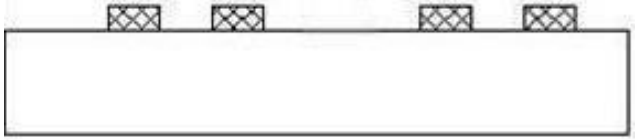
S1813

Cr/Ag

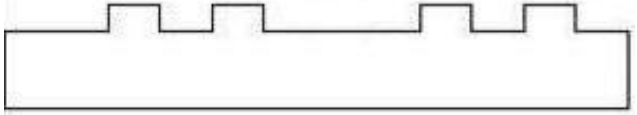
Ni

(1) 清洗矽晶片，並烤乾

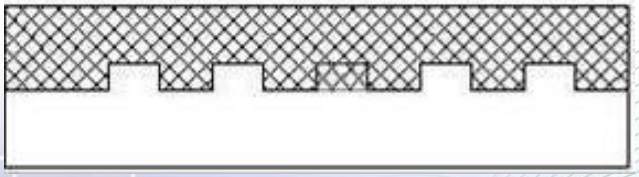
(2) 光阻塗佈，並軟烤



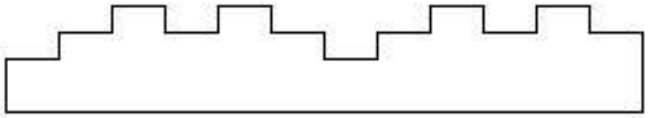
(3) 曝光顯影



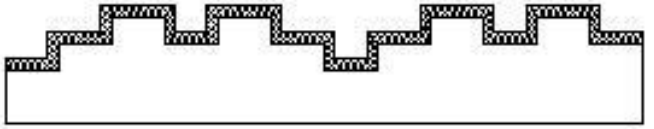
(4) 蝕刻第一層



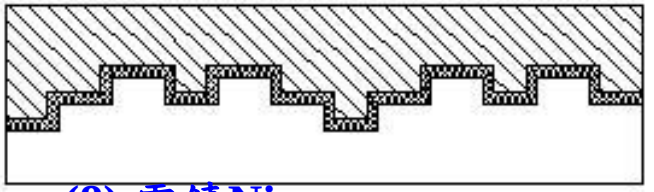
(5) 二次塗佈光阻



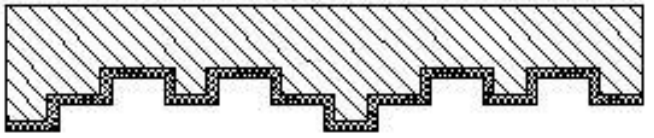
(6) 蝕刻第二層



(7) 蒸鍍Cr/Ag

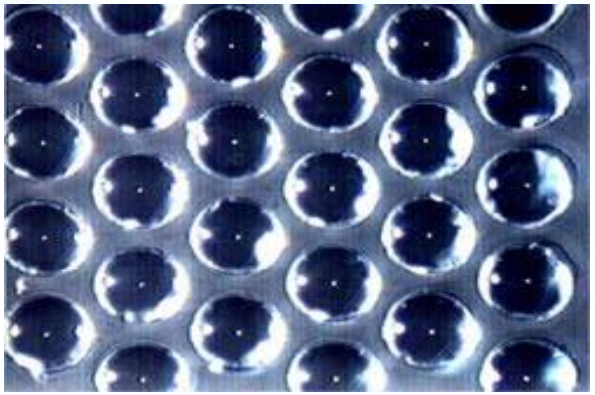


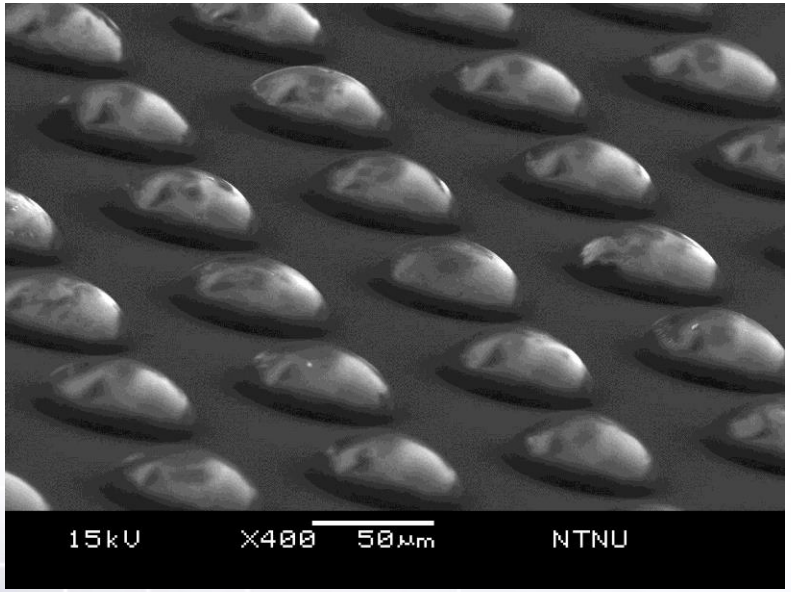
(8) 電鑄Ni

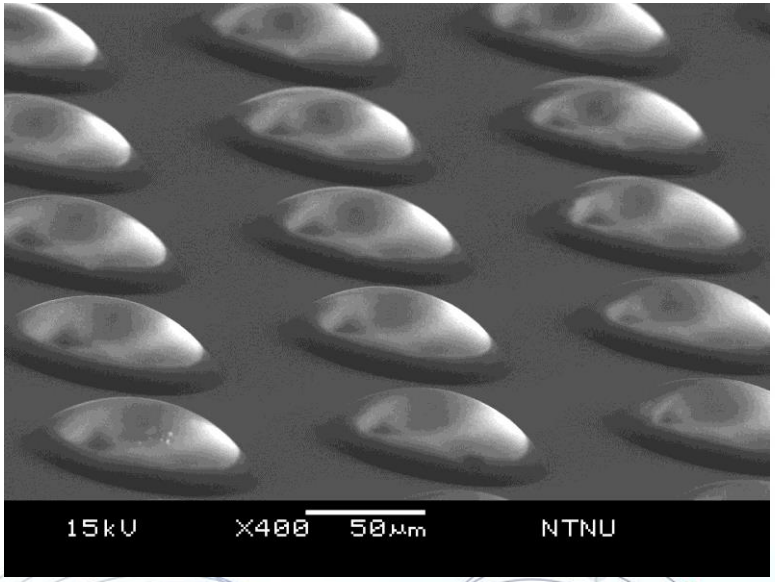


(9) Ni模

微透鏡陣列製程

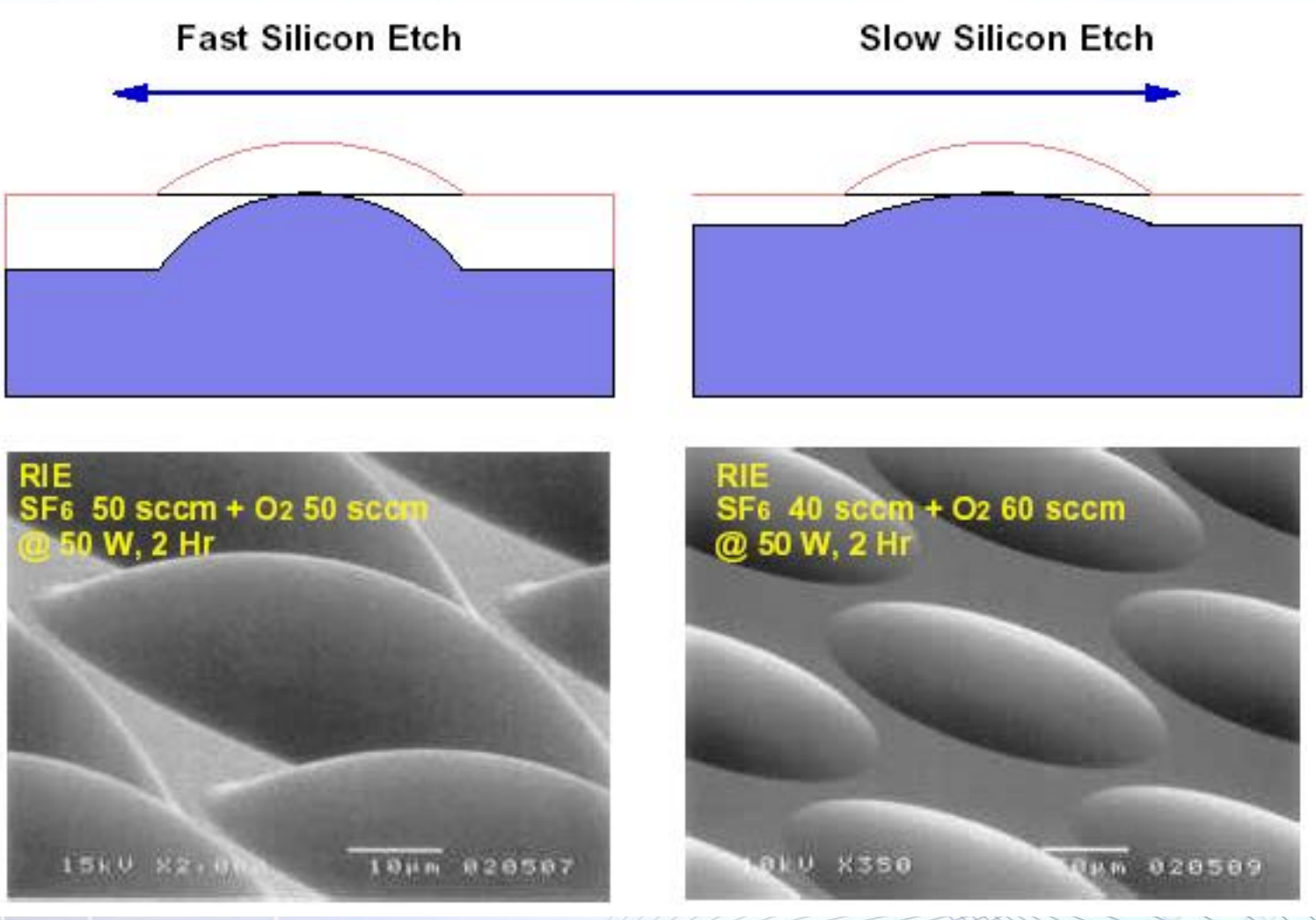




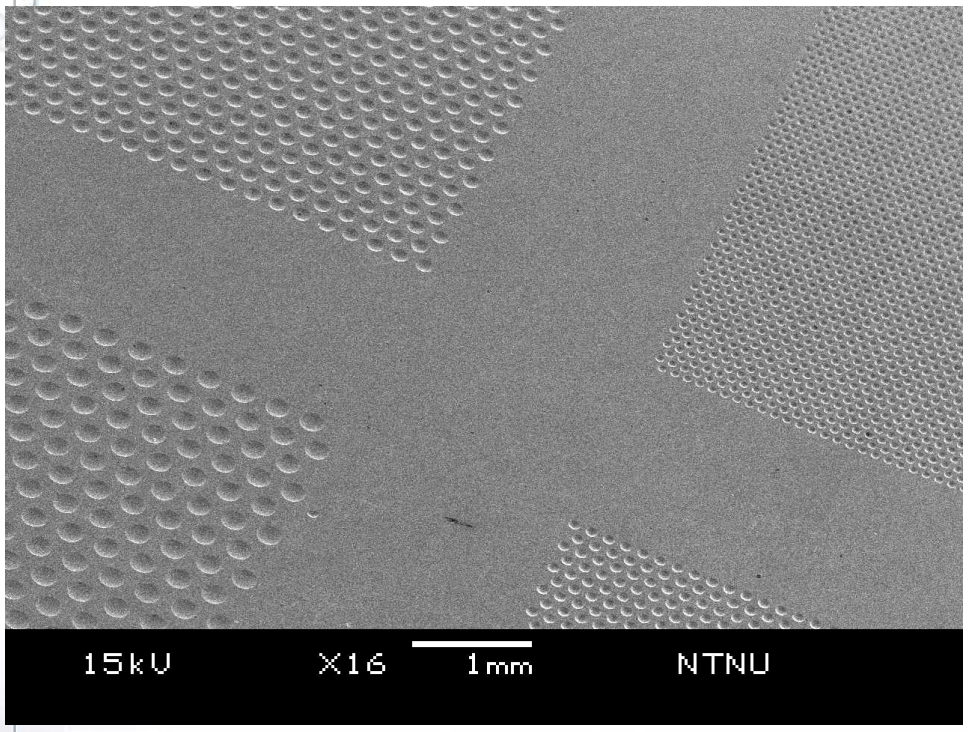


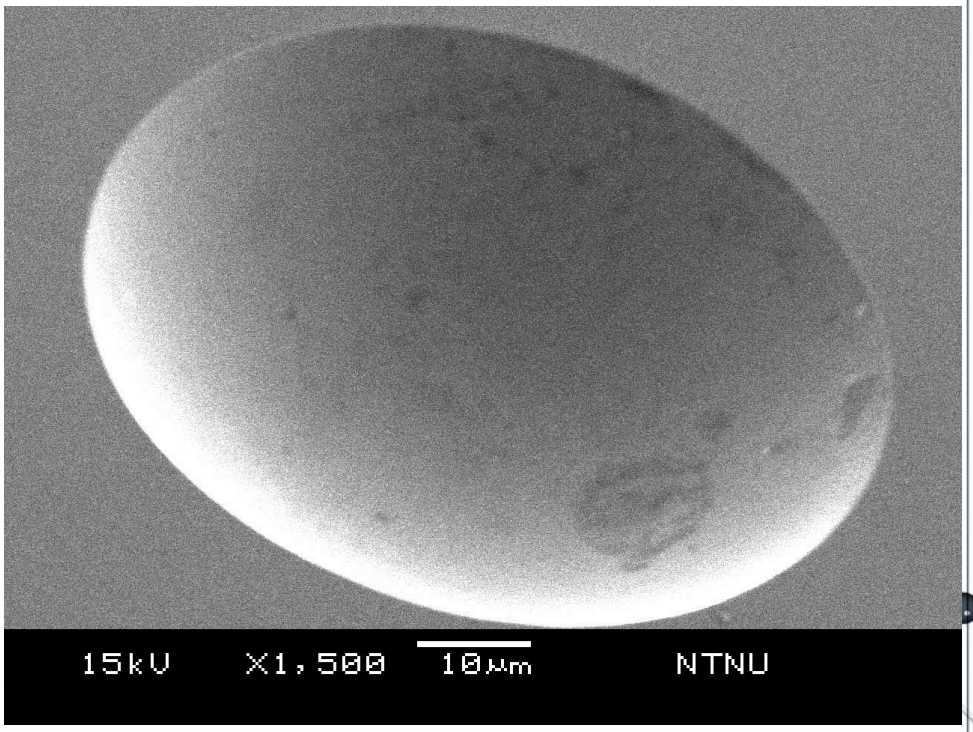
微透鏡陣列

Transferring Photoresist Pattern into Silicon

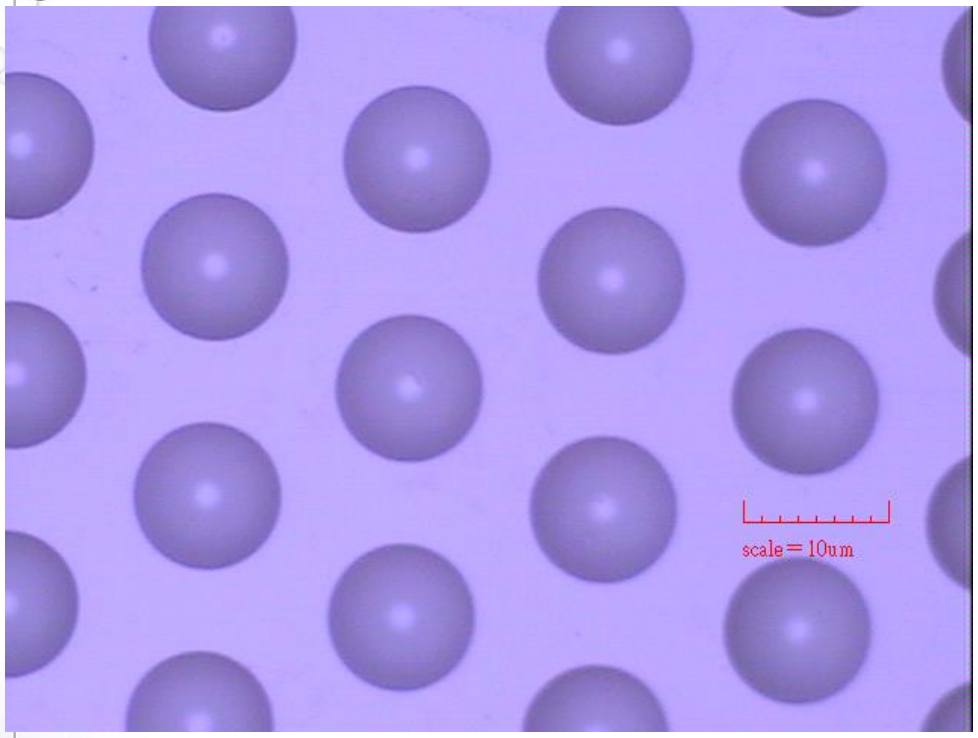


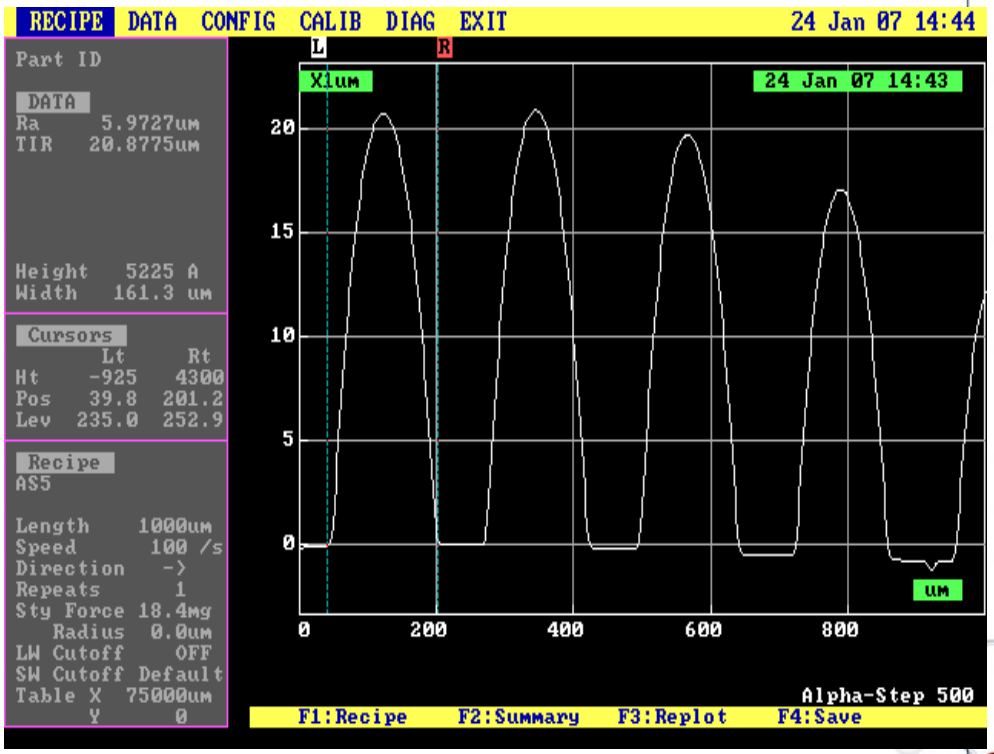
電鑄後的SEM圖





微透鏡陣列壓模成果


scale＝10um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Part ID
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TIR 20.8775um
Height 5225 A
Width 161.3 um
Cursors
Lt Rt
Ht -925 4300
Pos 39.8 201.2
Lev 235.0 252.9
Recipe
AS5
Length 1000um
Speed 100 /s
Direction ->
Repeats 1
Sty Force 18.4mg
Radius 0.0um
LW Cutoff OFF
SW Cutoff Default
Table X 75000um
Y 0
L
R
Xlum
24 Jan 07 14:43
20
15
10
5
0
0
200
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600
800
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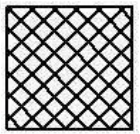
Alpha-Step 500
F1:Recipe F2:Summary F3:Replot F4:Save

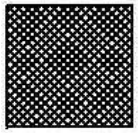
微透鏡模仁製作流程圖

Si



AZ4620

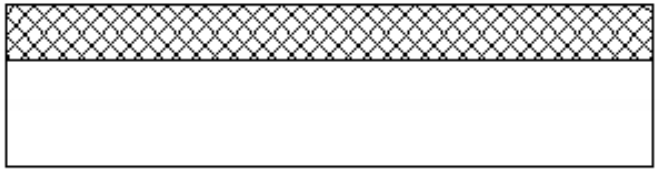
Reflow



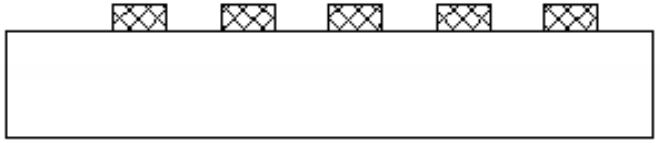
Cr/Ag

Ni

(1) 清洗矽晶片，並烤乾



(2) 光阻塗佈，並軟烤

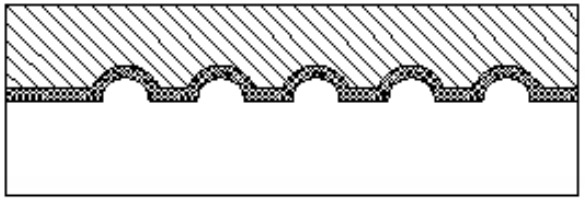


(3) 曝光顯影

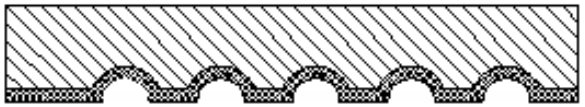
(4) 光阻熱熔

(5) RIE蝕刻

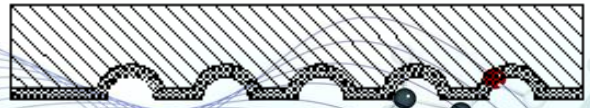
(6) 蒸鍍Cr/Ag



(7) 電鑄Ni

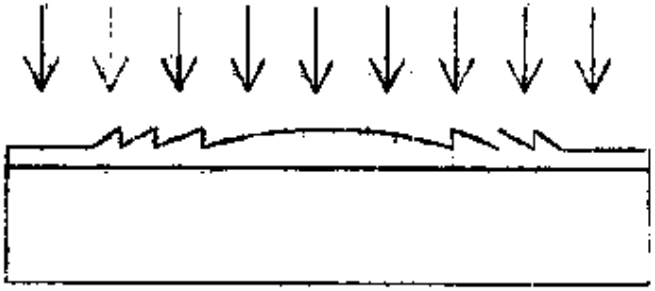


(8) 脫膜

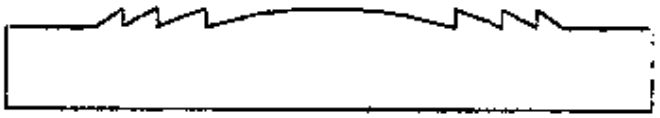


(9) Ni模

Lens profile in resist on glass or silicon

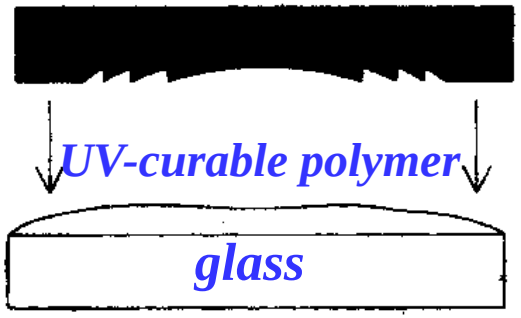


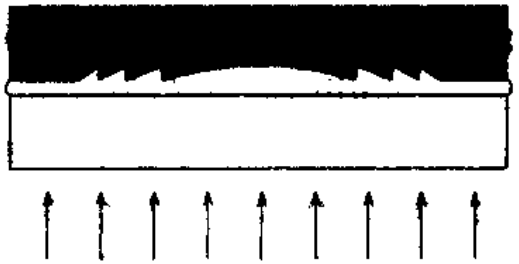
Ion etching



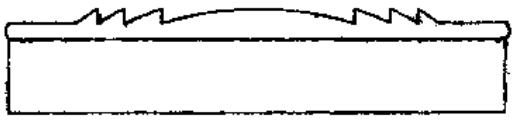
Lens profile etched into glass or silicon

Ni stamper

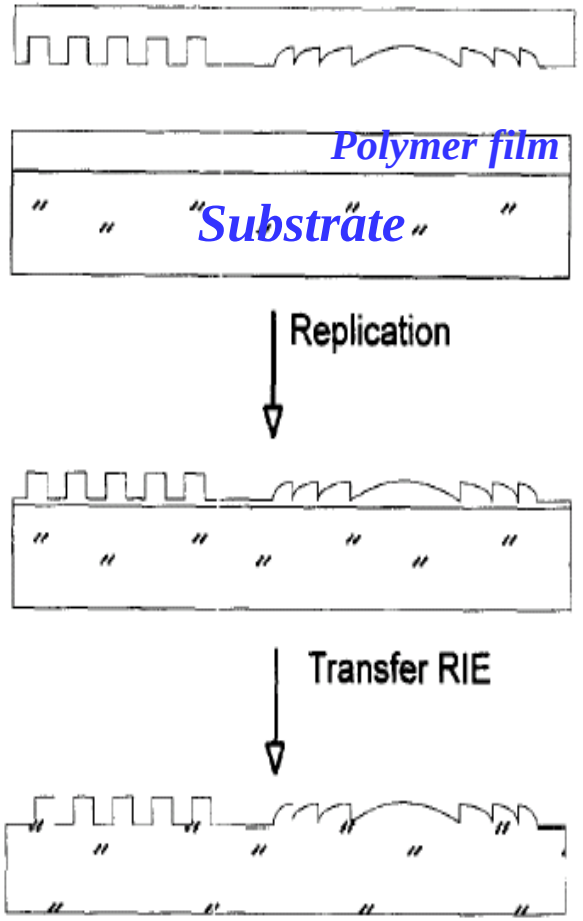




UV exposure



Ni stamper



Conclusions

Micro/Nano-Machines

(機械："kikai")

create

Macro-Opportunities

(機會："kikai")

By Dr. Osamu Tabata, Ritsumeikan University

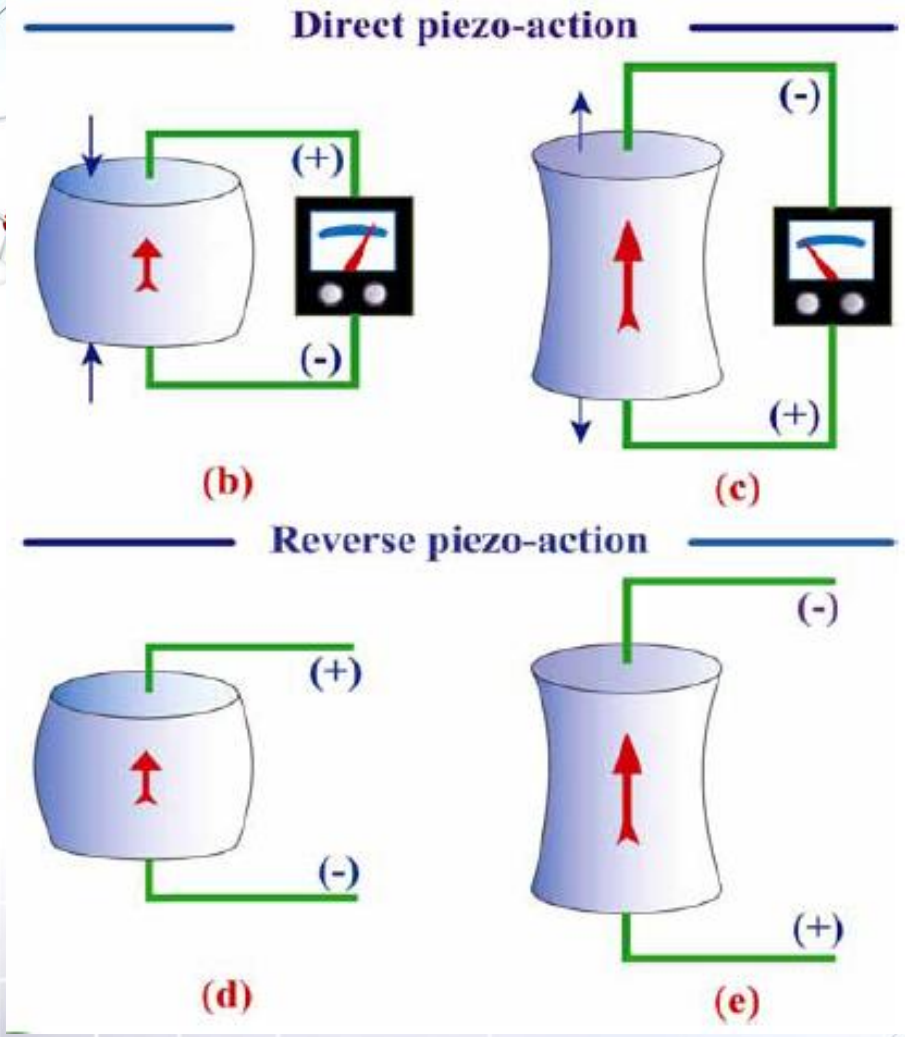
Keep on moving !

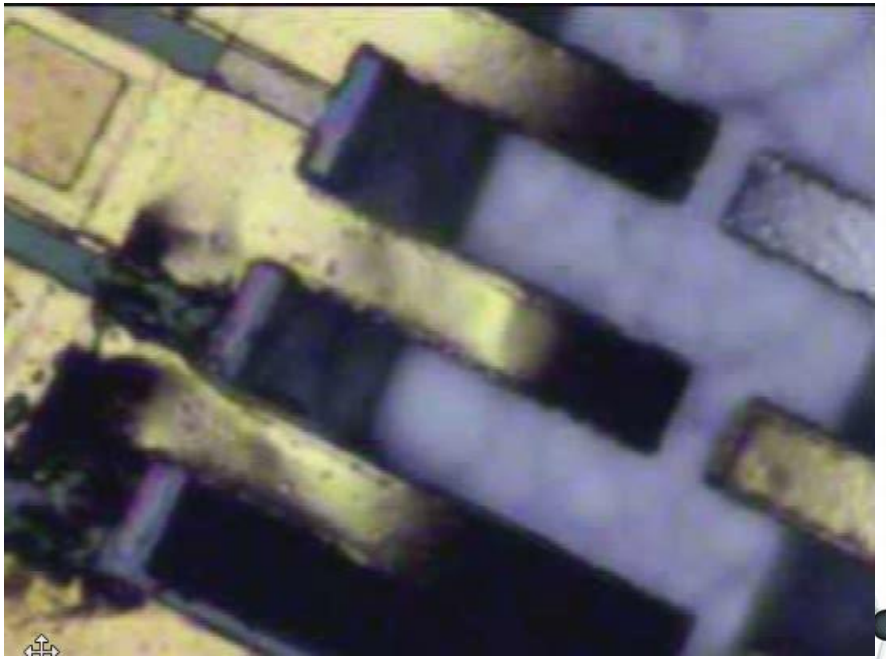
By Dr. Yang, National Taiwan Normal University

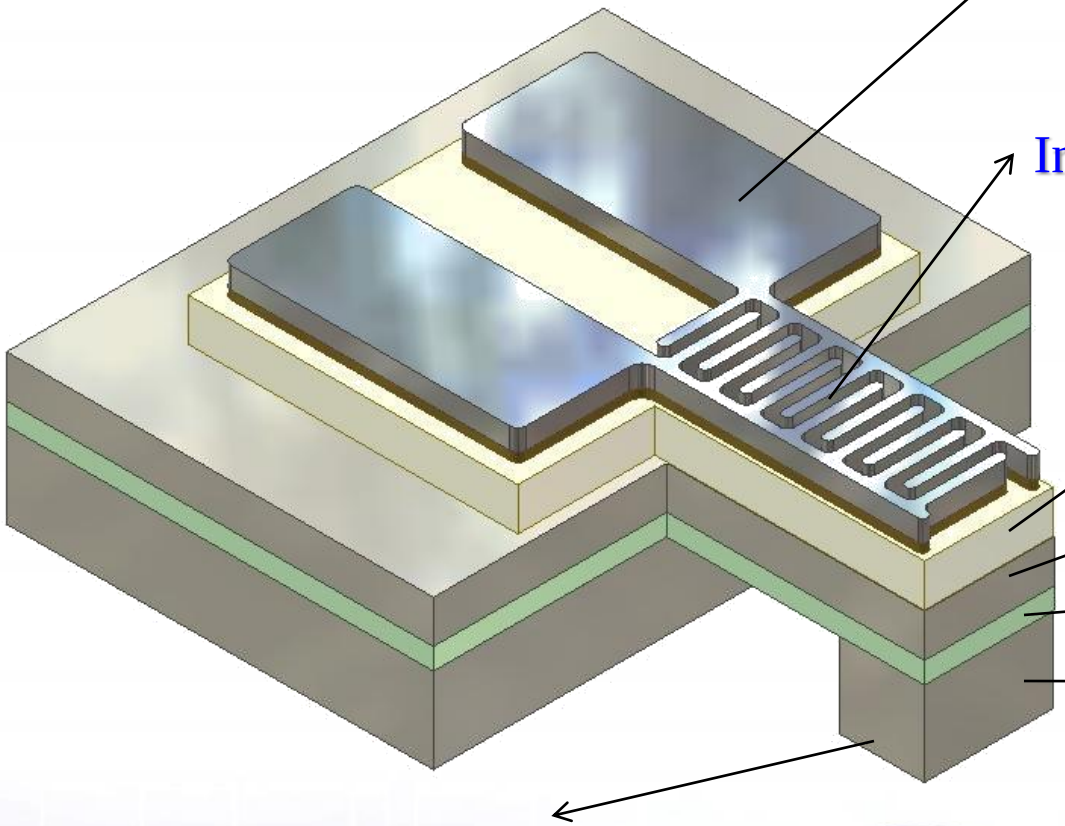
敬請批評與指教

Thank you for your attention!

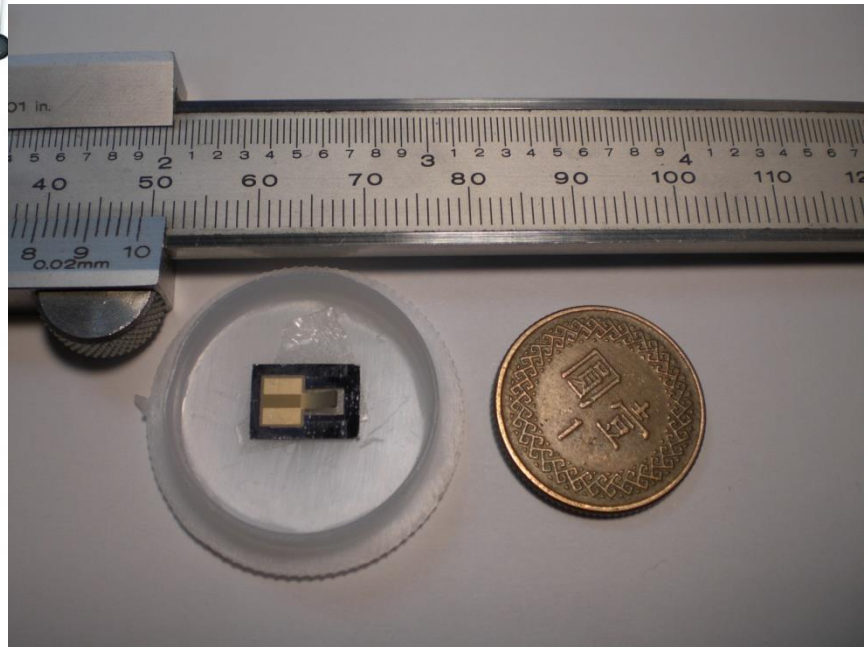
Piezoelectric

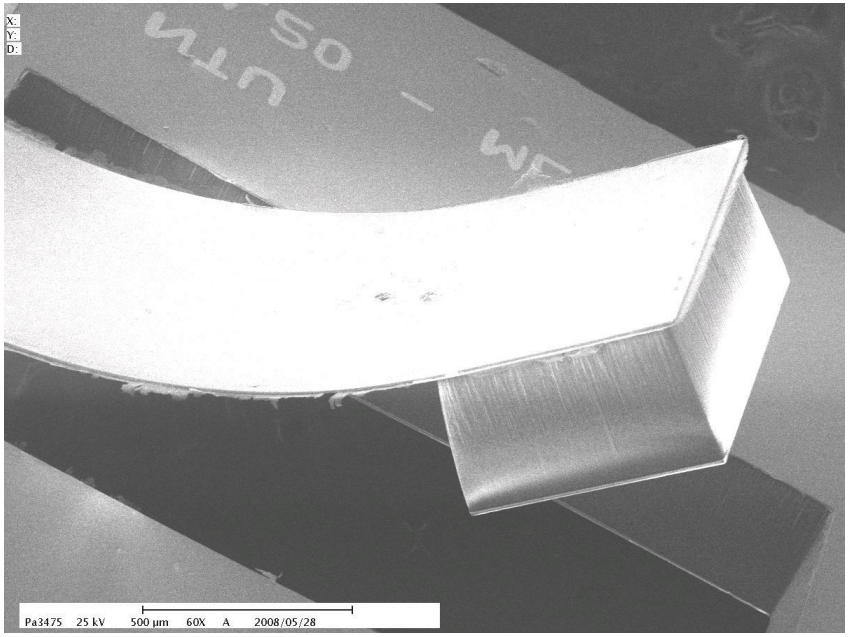






The finished d33 mode piezoelectric MEMS generator.





The finished d33 mode piezoelectric MEMS generator.